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UNIVERSITÉ DE MONTRÉAL

ON-CHIP INTEGRATED FUNCTIONAL NEAR INFRA-RED SPECTROSCOPY (fNIRS) PHOTORECEIVER FOR PORTABLE BRAIN IMAGING

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Cette thèse intitulée:

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DEDICATION

To My Beloved Family and Friends

and All My Former Professors and Teachers…

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RÉSUMÉ

L'imagerie cérébrale fonctionnelle utilisant la Spectroscopie Fonctionnelle Proche-Infrarouge (SFPI) propose un outil portatif et non invasif de surveillance de l'oxygénation du sang. SFPI est une technique de haute résolution temporelle non invasive, sûr, peu intrusive en temps réel et pour l'imagerie cérébrale à long terme. Il permet de détecter des signaux hémodynamiques à la fois rapides et neuronaux ou lents. Outre les avantages importants des systèmes SFPI, ils souffrent encore de quelques inconvénients, notamment d'une faible résolution spatiale, d'un bruit de niveau modérément élevé et d'une grande sensibilité au mouvement. Afin de surmonter les limites des systèmes actuellement disponibles de SFPI non-portables, dans cette thèse, nous en avons introduit une nouvelle de faible puissance, miniaturisée sur une puce photodétecteur frontal destinée à des systèmes de SFPI portables. Elle contient du silicium photodiode à avalanche (SiAPD), un amplificateur de transimpédance (TIA), et « Quench-Reset », circuits mis en œuvre en utilisant les technologies CMOS standards pour fonctionner dans les deux modes : linéaire et Geiger. Ainsi, elle peut être appliquée pour les deux fNIRS : en onde continue (CW- SFPI) et pour des applications de comptage de photon unique. Plusieurs SiAPDs ont été mises en œuvre dans de nouvelles structures et formes (rectangulaires, octogonales, double APDs, imbriquées, netted, quadratiques et hexadecagonal) en utilisant différentes techniques de prévention de la dégradation de bord prématurée. Les principales caractéristiques des SiAPDs sont validées et l'impact de chaque paramètre ainsi que les simulateurs de l'appareil (TCAD, COMSOL, etc) ont été étudiés sur la base de la simulation et de mesure des résultats. Proposées SiAPDs techniques d'exposition avec un gain de grande avalanche, tension faible ventilation et une grande efficacité de détection des photons dans plus de faibles taux de comptage sombres. Trois nouveaux produits à haut gain, bande passante (GBW) et à faible bruit TIA sont introduits basés sur le concept de gain distribué, d'amplificateur logarithmique et sur le rejet automatique du bruit pour être appliqué en mode de fonctionnement linéaire. Le TIA proposé offre une faible consommation, un gain de haute transimpédance, une bande passante ajustable et un très faible bruit d'entrée et de sortie. Le nouveau circuit mixte trempe-reset (MQC) et un MQC contrôlable (CMQC) frontaux offrent une faible puissance, une haute vitesse de comptage de photons avec un commandable de temps de hold-off et temps de réinitialiser. La première intégration sur puce de SiAPDs avec TIA et Photon circuit de comptage a été démontrée et montre une amélioration de l'efficacité de la photodétection, spécialement en ce qui concerne la sensibilité, la consommation d'énergie et le rapport signal sur bruit.

ABSTRACT

Optical brain imaging using functional near infra-red spectroscopy (fNIRS) offers a direct and noninvasive tool for monitoring of blood oxygenation. fNIRS is a noninvasive, safe, minimally intrusive, and high temporal-resolution technique for real-time and long-term brain imaging. It allows detecting both fast-neuronal and slow-hemodynamic signals. Besides the significant advantages of fNIRS systems, they still suffer from few drawbacks including low spatial-resolution, moderately high-level noise and high-sensitivity to movement. In order to overcome the limitations of currently available non-portable fNIRS systems, we have introduced a new low-power, miniaturized on-chip photodetector front-end intended for portable fNIRS systems. It includes silicon avalanche photodiode (SiAPD), Transimpedance amplifier (TIA), and Quench-Reset circuitry implemented using standard CMOS technologies to operate in both linear and Geiger modes. So it can be applied for both continuous-wave fNIRS (CW-fNIRS) and also single-photon counting applications. Several SiAPDs have been implemented in novel structures and shapes (Rectangular, Octagonal, Dual, Nested, Netted, Quadratic and Hexadecagonal) using different premature edge breakdown prevention techniques. The main characteristics of the SiAPDs are validated and the impact of each parameter and the device simulators (TCAD, COMSOL, etc.) have been studied based on the simulation and measurement results. Proposed techniques exhibit SiAPDs with high avalanche-gain (up to 119), low breakdown-voltage (around 12V) and high photon-detection efficiency (up to 72% in NIR region) in additional to a low dark-count rate (down to 30Hz at 1V excess bias voltage). Three new high gain-bandwidth product (GBW) and low-noise TIAs are introduced and implemented based on distributed-gain concept, logarithmic-amplification and automatic noise-rejection and have been applied in linear-mode of operation. The implemented TIAs offer a power-consumption around 0.4 mW, transimpedance gain of 169 dBΩ, and input-output current/voltage noises in fA/pV range accompanied with ability to tune the gain, bandwidth and power-consumption in a wide range. The implemented mixed quench-reset circuit (MQC) and controllable MQC (CMQC) front-ends offer a quench-time of 10ns, a maximum power-consumption of 0.4 mW, with a controllable hold-off and reset-times. The on-chip integration of SiAPDs with TIA and photon-counting circuitries has been demonstrated showing improvement of the photodetection-efficiency, specially regarding to the sensitivity, power-consumption and signal-to-noise ratio (SNR) characteristics.

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LIST OF ABBREVIATIONS

ABC	Automatic (adaptive) bias control
ADC	Analog to digital converter
AGC	Automatic gain control
APD	Avalanche photodiode
AQC	Active quenching circuit
AQRC	Active quench and reset circuit
BER	Bit error rate
BW	Bandwidth
CF-TIA	Capacitive-feedback TIA
CG-TIA	Common-gate TIA
CMC	Canadian microelectronic corporation
CMQR	Controlled Mixed Quench-Reset
CMOS	Complementary metal-oxide semiconductor
CMRR	Common Mode Rejection Ratio
CSF	Cerebrospinal fluid
CW	Continuous wave
DA	Discrete Amplifier
DAD	Dual APD detector
DGTIA	Distributed-gain TIA
DMUX	Demultiplexer
DTMOS	Dynamic-threshold voltage MOSFET
EEG	Electro-encephalography
FD	Frequency-domain

FEC	Forward error correction
fMRI	Functional magnetic resonance imaging
fNIRS	Functional near infrared spectroreflectometry
GBW	Gain-bandwidth product
GM-APD	Geiger-mode avalanche photodiode
GM-SiAPD	Geiger-mode silicon avalanche photodiode
GPC	Gated photon-counting
HCI	Human-computer interface
HPF	High-Pass Filter
ICMR	Input common-mode range
LA	Limiting Amplifier
LED	Light-emitting diode
LogTIA	Logarithmic transimpedance amplifier
LPF	Low-Pass Filter
MEG	Magneto-encephalography
MGPC	Multi-Gate Photon-Counting
MQC	Mixed quenching circuit
NAF	Negative Avalanche Feedback
NEP	Noise equivalent power
NIR	Near-infrared
NSDD	Null source-detector distance
NSDS	Null source-detector separation
OTA	Operational Transconductance Amplifier
PD	normal PIN photodiode

PDE	Photon Detection Efficiency
PDP	Photon Detection Probability
PET	Positron emission tomography
PQ	Passive quenching
PQC	Passive quenching circuit
PMT	Photomultiplier tubes
RF	Radio frequencies
RF-TIA	Resistive-feedback TIA
SAM	Separate absorption multiplication
SAPD	Single-photon avalanche photodiode
SDD	Source-detector distance
SiAPD	Silicon CMOS avalanche photodiode
SNR	Signal-to-noise ratio
SPAD	Single-photon avalanche photodiode
TCSPC	Time-correlated single-photon counting
TD	Time-domain
TIA	Transimpedance amplifier
TR	Time-resolved

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CHAPTER 1 INTRODUCTION

1.1 Motivation and General Background

The circulatory system is one of the main building blocks of the human body which is controlled by both brain and heart. Due to the importance of these two critical organs, monitoring neurovascular dynamics is of great value for clinical and brain-machine interface (BMI) applications, and is a challenge in biomedical imaging endeavors. The neurovascular diseases are of great social impact, as they are the frequent cause of death in the world and the most frequent cause of disability in adults [1], [2]. Stroke (cerebrovascular accident or CVA) is a leading cause of adult disability and the third leading cause of death in the United States, causing death off around 157,000 people per year with an estimated society cost of 58 billion dollars only in 2006 [3]. The medical imaging techniques have widespread applications include diagnosing diseases. Thanks to new technologies such as radio-frequency (RF), electromagnetic, ultrasound, and infrared detection, the new bio-imaging systems are applied in different aspects and activities of neurological and cardiovascular monitoring and treatment [1].

The use of diagnostic brain imaging has increased dramatically over the past decade. Table 1.1 shows the comparison of the most common brain imaging techniques [1]. Common brain monitoring systems are bulky, non-portable and invasive and require sophisticated and expensive hardware and software tools (e.g. a typical 1.5 Tesla MRI cost is up to 3M$) [4]. The commonly used non-invasive brain imaging techniques are electro-encephalography (EEG), positron emission tomography (PET), functional magnetic resonance imaging (fMRI), and functional near-infrared spectroscopy (fNIRS) [5]. Only EEG and fNIRS can be realized using equipment that is small and light enough to be worn continuously while allowing body movements which is important especially for neonates, long-term monitoring and BMI applications. Some portable EEG systems have been developed for brain imaging [6], however EEG is not ideal for human-computer interface (HCI) [7], it is susceptible to artifacts from eye and facial movement, as well as by electronic devices, it requires gel in the participant's hair, and a long set-up time, and it is not spatially determined [8].

Table 1.1: Comparison of various brain imaging techniques.

	Image/Data Quality	Temporal Resolution	Spatial Resolution	Mobility Tolerance	Scale	Safety	Cost
MRI	High	Low (~30s)	Very-High (3-6 mm)	Medium	Bulky	High	High
fMRI	High	Low (~30s)	Very-High (3-6 mm)	Medium	Bulky	High	High
X-Ray	Low	Medium (1s-10s)	Very-High (1 mm)	Low	Bulky	Low*	Low
CT-Scan	Low	Medium (10s)	Very-High (1mm)	Low	Bulky	Low*	Low
Ultrasound	Low	Hi (~1ms)	Depends on the probe element width	Low	Medium	Very-High	Low
PET	High	Low (30s-40s)	High (5mm)	Very-high	Bulky	Low*	Very-high (1-2M$)
SPECT	Medium	Very-Low	Medium (1cm)	Medium	Bulky	Low	High (0.5-1M$)
MEG	Medium	Very-High (~1ms)	Low (1cm - 2cm)	Medium	Bulky	Low	High
EEG/ERP	Medium	Very-High (~1ms)	Medium (1cm)	Low	Small	High	Low
fNIRS	High	High (0.5s-1s)	Low-Medium (0.5cm-2cm)	Medium	Small	Very-High	Very-low

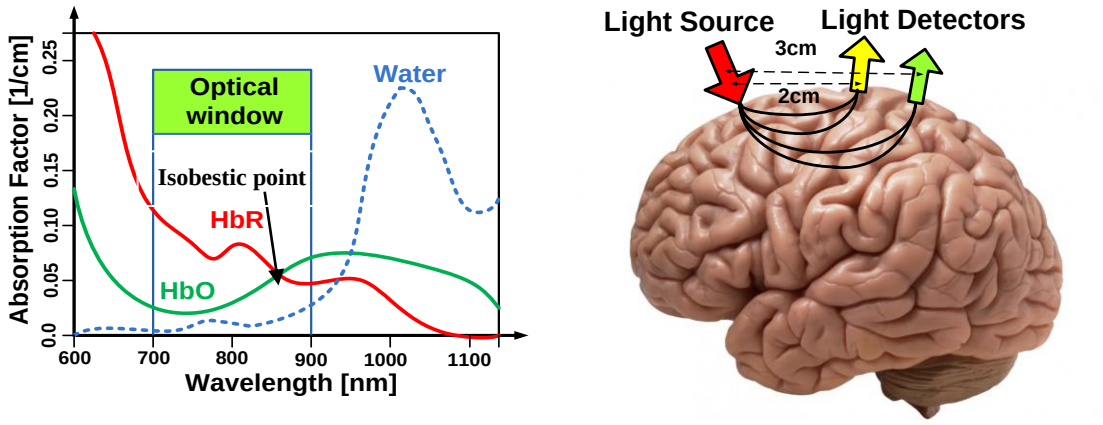
*Ionizing Radiation

In contrast to the other bulky and high-voltage brain-imaging systems suffering from electromagnetic interferences and slight movement artifacts, fNIRS is relatively robust against motion artefact, compact (portable), low-voltage and immune to electromagnetic interferences with the advantages of ease of use, low-absorption (no heating), and low-energy (no ionization) [8]. It offers a direct non-invasive, minimally intrusive and safe tool for real-time and long-term continuously monitoring of biological signals (such as HbO, HbR and HbT) with high temporal-resolution and low-cost. fNIRS obtain information on cerebral oxygenation, activation and blood volume, not otherwise obtained with any single method and at a remarkably low-cost. It can be considered as a diagnosis and investigation technique for different neurological diseases, such as, stroke and epilepsy seizures that require continuous monitoring of patients at the hospital, which is a costly endeavor. It is a potential neuroimaging technique that can non-invasively monitor the rapid changes in both fast-neuronal (with ms temporal-resolution) and slow-hemodynamic signals (regional cerebral blood volume and tissue oxygenation).

Since cerebral blood volume and tissue oxygenation are indirect indicators of neuronal activity, such imaging information is of great value in the understanding, evaluation, and treatment of the common neurological diseases such as stroke and epileptic seizures. It is the best choice for Neonatology and auditory studies. NIRS can also be applied in light detection and ranging (LIDAR), photon-counting, fiber-optic communication, brain-computer interface, tele-control by thought, brain imaging (epilepsy, seizure, migran, schizophernia, credibility assessment, lie detection), human performance assessment, depth of anesthesia monitoring, pain assessment, virtual reality, neurorehabilitation, autism, breast cancer screening, and muscle oxygenation.

All these advantages have made NIRS the system of choice for neuroimaging and a hot topic of research towards developing a miniaturized and portable system for real-time brain imaging applications. Work is going on in different research groups to improve the performance of NIRS system [9], [10], [11]. However, to date the realization of this potential has not materialized with current commercial devices due to high energy-consumption and size issues of the fNIRS photodetector. The Imaginc group of Polytechnique Montreal is leading the development of a portable fNIRS system for real-time brain imaging. This thesis covers the design and implementation of the main building blocks of a portable fNIRS photoreceiver including avalanche photodiode, transimpedance amplifier and photon-counting circuits.

In fNIRS, the brain tissue is penetrated by near-infrared (NIR) radiation and the reflected signal is observed to investigate the brain neurovascular activities. In NIR range (650nm-950nm), water has relatively low absorption while oxy- and deoxy-hemoglobin have high absorption (Figure 1.1 (a)). Due to these properties, NIR light can penetrate biological tissues in the range of 0.5-3 cm allowing investigation of relatively deep brain tissues, and ability to differentiate between healthy and diseased tissues based on their optical properties (Figure 1.1 (b)). When light enters a tissue, its propagation is mainly governed by two physical phenomena, i.e., light absorption and scattering.



(a) (b)

Figure 1-1: The NIR optical window (a), and the banana shape path of light between optodes in different deparation distances (b).

There are certain substances in human tissues for which the spectra within the NIR wavelengths are well defined. Some of these absorbers such as water, melanin, and bilirubin do not change in concentration with time. But concentrations of some other absorbers such as oxygenated hemoglobin (HbO) and deoxy-hemoglobin (HbR) are strongly related to the tissue oxygenation and metabolism. Thus the absorption changes can provide clinically useful physiological information. The range from 700 nm to 900 nm called optical window (also called Therapeutic or near infrared window) is defined which is considered useful for the non-invasive NIR measurements. The NIRS is based on the Beer-Lambert law that explains the light attenuation (A) when passes through an absorbing medium as follow:

$$I(L) = I(0)\, e^{-\mu_a L} \Rightarrow A = \mu_a\, L = \varepsilon\, CL = \ln\left(\frac{I(0)}{I(L)}\right) \qquad (1.1)$$

where I is the light intensity, L (called path-length) is the distance between the light entrance points and its exit point (source-detector distance), C is the concentration, μ_a is the absorption coefficient of the medium, and ε is the molar absorption coefficient. For a medium having more than one absorbing compounds, overall attenuation is the linear sum of individual contributions:

$$\mathrm{A} = \ln\left(\frac{I(0)}{I(L)}\right) = (\varepsilon_1\, C_1 + \varepsilon_2\, C_2 + \varepsilon_3\, C_{31} + \cdots + \varepsilon_n\, C_n)\, L \qquad (1.2)$$

For human tissues, however, absorption is not the only phenomena. Light scattering also exists and is rather a dominant phenomenon. As scattering changes the optical path-length of the light propagation, absorption characteristics of the medium are difficult to quantify due to light scattering. Thus, Beer-Lambert's law was modified to be applicable in the human tissue. The modified Beer-Lambert's Law is given by:

$$\mathrm{A} = \ln\left(\frac{I(0)}{I(L)}\right) = \varepsilon CL.DPF + G = \mu_a\, L.DPF + G \qquad (1.3)$$

where G is the term added to compensate for scattering losses, and DPF is the differential path-length factor. The two main chromophores in tissue for the NIR window are HbR and HbO. Thus the absorption coefficients at two wavelengths can be given by:

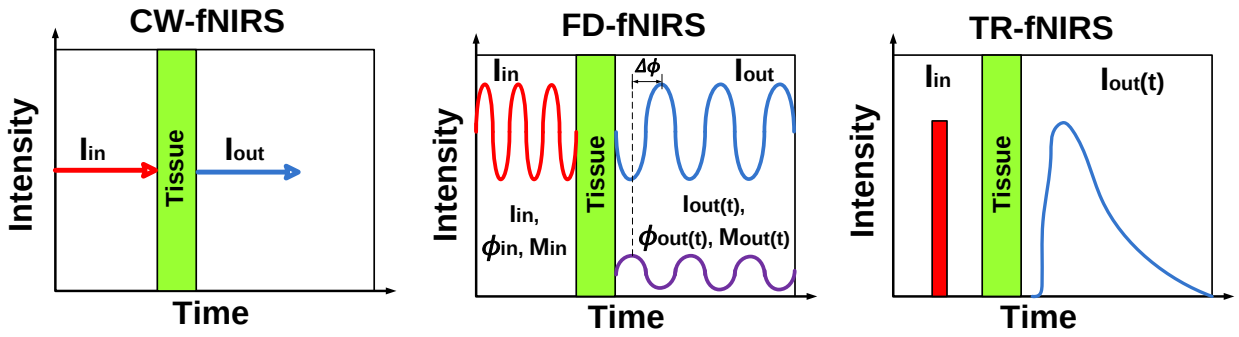
$$\begin{bmatrix}\mu_a(\lambda_1)\\ \mu_a(\lambda_2)\end{bmatrix} = \begin{bmatrix}\varepsilon_{HbR}(\lambda_1) & \varepsilon_{HbO}(\lambda_1)\\ \varepsilon_{HbR}(\lambda_2) & \varepsilon_{HbO}(\lambda_2)\end{bmatrix} \times \begin{bmatrix}HbR\\ HbO\end{bmatrix} \qquad (1.4)$$

The wavelengths should be selected properly to minimize the cross-talk between HbR and HbO. Usually 2 different wavelengths are chosen in either sides of isobestic point where the absorption are equal (eg. 780nm & 870nm). More wavelengths can differentiate between more chromophores such as water, lipid, melanin, cytochrome c oxidos (C_tO_x), HbR and HbO.

There are currently three fundamental types of NIR instruments used for probing the neurovascular response. A qualifier to each of these systems is its measurement geometry, which can be either transmission geometry or a reflective geometry. These three main types of fNIRS techniques which impose applying different types of instrumentation are:

(1) Continuous-wave (CW) or continuous-intensity (CI) fNIRS:

In this technique (Figure 1.2(a)), a continuous-wave light source is used and the intensity variation (ΔI) of the input continuous NIR light are measured at the output to determine only the relative changes. However, using iterative measurements by changing a variable (such as light intensity, wavelength, source-detector distance), the quantitative and absolute variation can also be determined. CW-fNIRS can determine the O2, cytochrome c oxidase (C_tO_x) and arterial hemoglobin saturation ($Sa{O_2}$) levels as critical vital signals [12].



(a) (b) (c)

Figure 1-2: Different types of NIRS systems: CW-fNIRS (a), FD-fNIRS (b), and TR-fNIRS (c)

(2) Intensity-Modulated (IM) or Frequency-Domain (FD) fNIRS:

This technique (Figure 1.2(b)) uses an intensity-modulated light source (usually at RF) and records the intensity (I(t)), the phase-shift (ϕ(t)), and the modulation-depth (or Modulation-Index: M(t)) at the output. Here the intensity (amplitude) of the applied continuous-wave source is modulated at a high radio frequency (~100MHz) or even lower frequencies using heterodyning (combining or mixing two frequencies to create a new desired frequency) to reduce the ADC complexity and improve the SNR. FD intrinsically yields more information than CW but due to high-noise level in phase data its sensitivity to cerebral hemodynamics is weak [13], [14]. Furthermore, the phase information (typically used to measure scattering) has not been shown to provide robust measures of cerebral hemodynamic variation [13].

(3) Time-Resolved (TR) or Time-correlated single-photon system (TCSPS):

It measures the temporal distribution of output light (I(t)) resulting from an ultrafast pulse (1-200 ps) input NIR light source (Figure 1.2(c)). Measurements at multiple wavelengths enable estimations of the concentrations of different absorbers. This technique, which is called the time-domain (TD) or time-pulsed NIRS, measures the time-of-flight (TOF) of photons and acquires information at all frequencies simultaneously at desired depth. CW and TD have the same contrast to noise ratio [13], but TD have a better contrast to background ratio and also better depth sensitivity and resolution with the cost of using more complicated circuitry and higher expense [13].

Towards developing a miniaturized and low-power portable fNIRS with low-cost, the CW-fNIRS would be a proper technique comparing to other bulky and high-power methods requiring more complicated circuits and extra building blocks. The typical CW-fNIRS system consists of NIR light source, photodetector, data acquisition module, control unit, and a processing block. The light source is placed on the surface of the head (scalp) and it generates light in the NIR range. Generally, the light sources used for NIRS system are either LEDs or laser diodes that emit NIR light with optical power within a range of 5 mW to 17 mW at discrete wavelengths (for example 735, 840, and 940 nm). In comparison to laser diodes, LEDs are easy to reproduce, less expensive, have lower-power and larger emitting regions, and longer lifetimes. The fNIRS photodetector front-end includes a photodetector that monitors the intensity of the reflected NIR signal, Quench–Reset circuit, Transimpedance Amplifier (TIA), Limiting Amplifier (LA), post amplifiers and filters. Although fNIRS is compact when compared to other brain imaging systems, but current commercially available NIRS devices are not miniaturized enough in order to be integrated with other wireless and portable medical imaging systems intended for bedside long-term brain monitoring. It also suffers from low-spatial resolution, high-level noise (movement, heart-rate, breathing rate, and low-frequency oscillations), susceptible to the internal and ambient light/temperature and bias voltage variations. Integrating the photodiode and corresponding circuitries on the same chip and on-chip multi-mode operation using smart CMOS image sensor concept has not been considered yet in the literature for fNIRS application. Using smart CMOS image sensor concept for fabrication of photodiode and photodetection circuitry and integrating them on the same chip with ability to works on different modes of operations, leads to a more compact and miniaturized design.

1.2 Background Theory of NIR Photodetectors (Theoretical framework)

1.2.1 Photodetection using Solid-State Materials

Semiconductor materials are used to fabricate photodetectors in order to detect photons (light) by their photo-sensitive characteristics and converting light into electricity. They can be used for direct detection of light, X-ray, gamma-rays, and particles such as electrons or neutrons. A photodiode is a reverse biased p−n junction as shown in Figure 1.3(a), whereas photons are absorbed everywhere and an electron-hole pair (EHP) is generated [15]. An electron in the

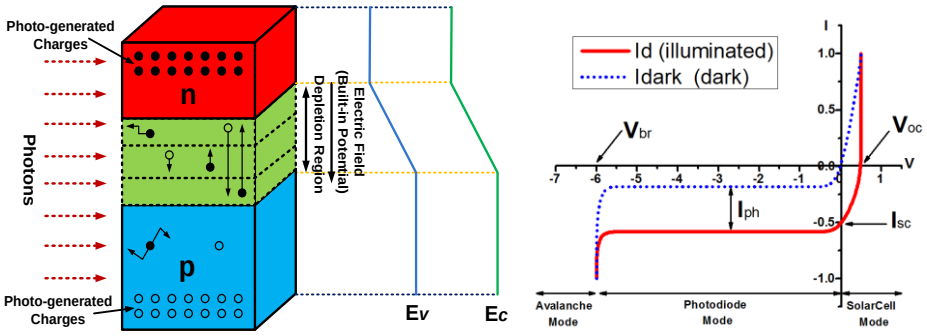
valence-band moves to the conduction band by absorbing energy from a photon upon generation of an EHP. Wherever the electric-field is present, electrons and holes are separated and transported in the opposite directions. Since the electric-field impact in a p−n junction occurs mostly in the depletion-region, the photocarrier-generation region is mostly confined to the depletion-region [16], [17]. Photodiodes can be produced from different materials such as Si, Ge, and III-V semiconductor compounds (obtained by combining group III elements (eg. Al, Ga, In) with group V elements (eg. N, P , As, Sb)) [18]. The direction of the incident-light and the p–n junction are often designed to be perpendicular to the p−n surface, instead of parallel to it. As shown in Figure 1.3(b), the photodiode has an I-V relation as[16]:

$$i = i_s \left[exp\left(\frac{eV}{k_B T}\right) - 1 \right] - i_p \tag{1.5}$$

The photocurrent (i_p) is proportional to the photon-flux [17]. The depletion-region in a p-n junction constructed in common CMOS technology is formed when the free holes/electrons in p-type/n-type materials diffuse across the junction. The holes diffuse into the n-type region and leave negatively charged ions in the p-type region, and the reverse applies to the electrons. This creats the depletion-region, which introduces a built-in potential to realize the photodetector. When a photon is absorbed anywhere close to the depletion-region, an electron-hole pairs (EHPs) separation occurs, and they move based on the direction of the electric-potential. Some photons reaching the depletion-region are absorbed, transferring their energy to the outer-shell electrons, and generating EHPs. The built-in potential then forces the holes to move toward the p-type region and the electrons toward the n-type region, and the moving holes and electrons result in an electrical current which is called the photocurrent. In order to utilize a p-n junction as a photodiode, its bias condition has to be carefully chosen. Three modes can be observed as plotted in Figure 1.3(b), which are the avalanche (large reverse-bias) [19], photodiode or image sensor (slight reverse-bias) [20] and solar-cell (forward-bias) [21] modes. The photodiode itself can be divided into three different regions of operation: open-circuit (photovoltaic), short-circuit, and reverse-biased (photoconductive-mode). When no light emits and the photodiode is in darkness, the current is negative but very close to zero which is mostly the thermally-activated diffusion-current of the junction and called the dark-current. When the photodiode is illuminated, the absolute net current becomes larger because of the photo-current (I_{ph}), which is subject to change with different amounts of electron-hole pairs generated and separated by the built-in potential

[15]. The increase of the photo-current is proportional to the incident-light intensity. Common silicon photodetectors are essentially PIN diodes that the incident-light generates EHPs in the depletion-region contributing to the reverse current. They can work on the same aforementioned three bias-regions as mentioned for p−n diodes. A PIN diode is a p−n junction with a wide intrinsic (lightly-doped) layer sandwiched between p and n layers, in which the p-type and n-type regions are typically heavily-doped because they are used for ohmic-contacts.

The wide intrinsic-region makes the PIN diode suitable for attenuators, fast-switches, photodetectors, and high-voltage power-electronics applications with the cost of less rectification. Using the intrinsic-region increases the depletion-width which increases the photon-absorption depth so improves the sensitivity to red and IR light. It also decreases the junction-capacitance, thereby reducing the RC-delay constant and the response-time of the photodetector [22]. The Photo-transduction in a photodiode is based on the EHPs generation when the energy of the incident-photon on the detector is greater than the bandgap of the material ($h\nu > E_g$). Due to the indirect-gap nature of silicon (where the photon-absorption transitions typically take place from valence to conduction band states which are above the conduction band edge), in silicon-based photodetectors, the maximum responsivity occurs on wavelengths which are substantially shorter than the bandgap-wavelength [17].



(a) (b)

Figure 1-3: The cross-section view of a p-n junction showing the photogeneration regions forming the photo-current and the band-diagram (a), and the I-V curves of a p-n junction photodiode in dark and illuminated conditions. E_v and E_c indicate the valence-band and the conduction-band energies, respectively. V_{oc} and I_{sc} are the open-circuit voltage and short-circuit current when there is illumination applied, respectively.

1.2.2 CMOS Image Sensors

In general, several concerns are linked to the pixel design, such as its size (pixel pitch), active region (where photons penetrate and get absorbed), and periphery effect. Smaller pixel size however offers a better image quality with more details but suffer from higher noise and crosstalk and also non-uniformity and sensitivity issues[15]. The CMOS image sensors (called pixel as well) construct the building blocks of many imaging devices like digital cameras and camera modules. A pixel usually includes a photodetector and the necessary circuit to perform signal readout and/or processing. Depending on the principle of pixel operation, it can be referred to as an active pixel sensor (APS), a passive pixel sensor (PPS), or a digital pixel sensor (DPS) as shown in Figure 1.4 and explained more in the details in [15],[23]. The PPS (the simplest and the earliest CMOS image sensor), includes a photodiode and a switch (row-select transistor). The APS (the most popular CMOS image sensor) usually equips the pixel with an active-device including an amplifier or a buffer and can be built with only one (or up to several) transistor(s). The DPS consists of more complex blocks, normally an analog-to-digital converter (ADC) and a memory cell, to perform in-pixel signal processing. The image sensors offer simple circuitry with high fill-factor (FF) and low-noise for different imaging applications, however their sensitivity and speed are limited. So for the low-level light detection (LLLD), the avalanche photodiode (APD) can be used as a highly-sensitive and fast alternative detector, which has been explained in follow.

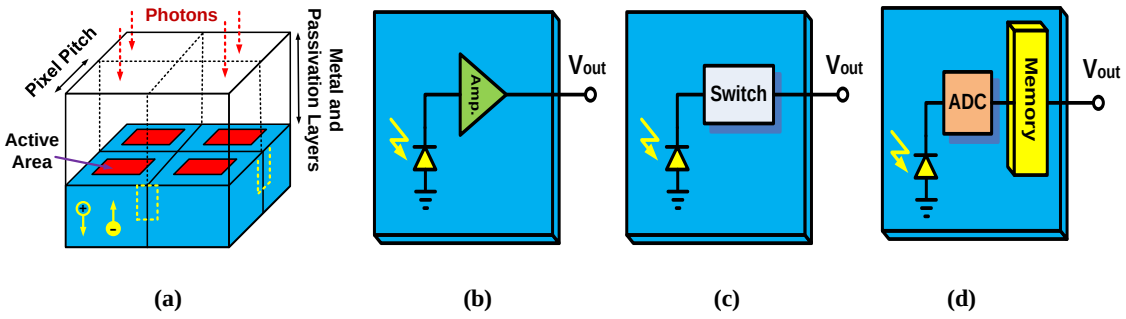
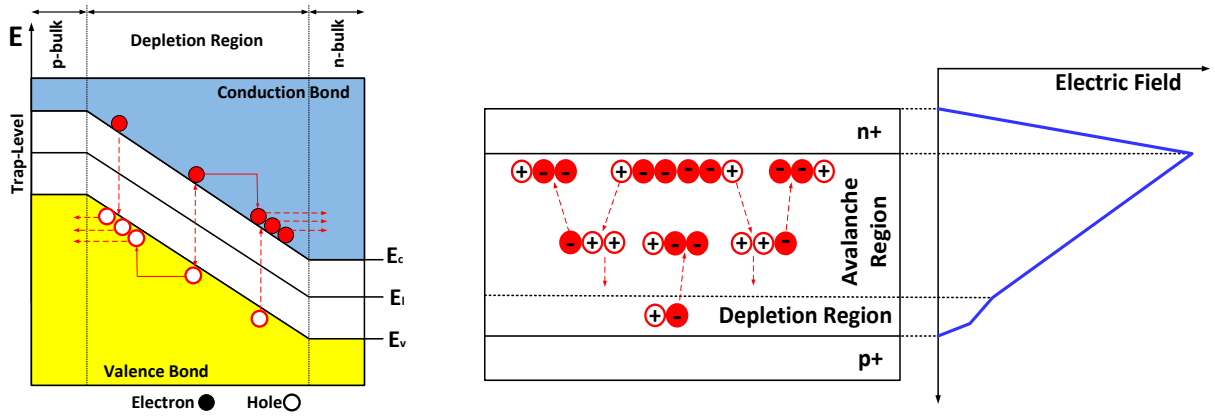


Figure 1-4: The illustration of concerns for pixel design (a), and the block diagrams of (b) APS, (c) PPS, and (d) DPS with in-pixel ADC structures.

1.2.3 Avalanche Photodiodes (APDs) and Impact Ionization

An avalanche photodiode is a strongly reverse-biased photodiode, where the applied electric-field across the junction, exceeds the critical value necessary to cause impact-ionization. The APD operation is based on conversion of the energy of photons into free charge carriers in the semiconductor bulk and their further multiplication via the process of impact-ionization. In contrast to the normal photodiodes, APD has a built-in region with very high electric-field. The charge-carriers by passing through this region acquire enough energy to produce more EHPs by impact-ionization and generate the avalanche of EHPs leading to a high output photo-current [24]. Figure 1.5 shows the principle operation of APDs. The absorbed photon, generates an EHP (an electron in the conduction-band and a hole in the valence-band). The electron ionizes an atom causes generating another EHP and so on. The required energy for an electron to ionize an atom is defined by relaxing the kinetic-energy of the electron in a high electric-field. The ability of an electron or a hole to trigger ionization is quantified by ionization-coefficients which increase with electric field and decrease with temperature. The increase of the ionization coefficient by electric-field is due to electron acceleration by electric-field and its decrease by increasing temperature is due to an increasing frequency of collision that decreases the probability of a carrier gaining enough energy to cause ionization.



(a) (b)

Figure 1-5: Representation of impact-ionization process in an APD (a), and the Energy Band diagram of a reverse biased PIN structure where impact-ionization process occurs as the electrons travels through the high electric-field region (b).

Widening the depletion-region (to maximizing the photon-detection probability) and reducing the thickness of the multiplication-region (to minimize the possibility of localized uncontrolled avalanches cause instabilities and microplasmas) elevate the APD performance and sensitivity [25], [26]. Maximizing the ratio of electrons to holes injected in the multiplying region reduces the noise generated in the APD due to the higher ionization-coefficient of electron [24]. The "Impact Ionization" is the process by which one energetic charge carrier (an electron or hole) can lose energy by the creation of other charge carriers (other EHPs) [27]. The electron and hole ionization coefficients (α and β respectively), determine the avalanche multiplication-gain and breakdown characteristics of APD [28], [29]. APDs use the impact ionization principle to detect and amplify very low light signals. In order to have a high-gain, low-noise APD, the ionization-rate for electrons and holes needs to be very different. The silicon has the largest ionization rate difference between electrons and holes among all semiconductors (electrons can ionize 50 times to 1000 times more readily than holes depending on the electric field amplitude), with the cost of its low cut-off wavelength around 1μm. So it is an ideal material to implement highly-sensitive and low-noise photodetectors. The probability for initiating impact ionization is quantified as the impact ionization coefficient. It is defined as the reciprocal of the average distance travelled by an electron or hole to produce an electron-hole pair. Materials with very different value for α and β, such as in silicon can create less impact ionization noise because only one type of carrier is dominant during the ionization process. The ionization coefficients (α and β) are strong function of electric field in the multiplication region. Electric field, however, also depends on the bias voltage, doping-profile, and the device geometry. Electron ionization is measured by shining light from the p+ side. Photon-excited electrons are injected into the intrinsic layer while holes are swept to the left. The hole-ionization is measured by illuminating light from the n+ side, injecting holes into the intrinsic layer. Wide bandgap semiconductors (such as GaAs) are associated with a high breakdown voltage. This is due to a larger electric field required to generate carriers through impact mechanism. InGaAs with narrow band gap is also a popular material in infrared detectors and some short wave infrared cameras. It also has lower multiplication noise than germanium when used as the active multiplication layer of an avalanche photodiode, and it also has a low breakdown-voltage [30], [31]. If an APD has the internal gain of M, for a single detected photon, the avalanche process produces M carriers [32]. The

maximum value of M is equal to α/β, in which α is the ionization coefficient of electrons and β is the ionization coefficient of holes. Increasing the avalanche-gain of M is achievable by widening the multiplication-region. A wider Multiplication-region increases the M (accompanied with a higher noise-level) and reduces the response-bandwidth. By further increasing the bias, an APD gain becomes virtually infinite. This biasing regime is known as Geiger-mode of operation and the APD called Single-Photon Avalanche Diode (SPAD). In this case a single electron can start the avalanche process until an external circuit (Quench circuit) limits the avalanche current and preventing the device damage. [33], [32].

1.2.4 Dark-Current and Tunneling

A dark-count is an avalanche event caused by non-photogenerated carriers, which as depicted in Figure 1.6(a), can be originated from: diffusion from neutral-regions, thermal-generation, release from a charge-trap, Shockley-Read-Hall (SRH) generation via impurities, or from band-to-band tunnelling in the depletion-region [34], [35]. Very-high electric-fields can also increase the dark-count rate (DCR), since the carrier-emission probability from generation centers is strongly enhanced by barrier-lowering, Frenkel-Poole effect and the photon-assisted tunneling [36]. The DCR can produce an output-pulse indistinguishable from the one originated by a detection-event. Dark-count noise increases with temperature, as the thermal carrier generation increases and so the probability of avalanche. The thermal-generation is strongly dependent on the fabrication process, which determines the concentration of traps, the breakdown-voltage and the avalanche probability. On the contrary, tunnelling-generation depends on the doping-profile and the bias-voltage, and its temperature dependence is weak [31]. Designing an APD with low-DCR is critical especially for photon-starved applications. However, a medium range noise can be acceptable as it is applied in current commercial imaging systems which can sustain relatively high DCRs (around few kHz) due to the relatively high-level of background noise [37].

The carrier transport in solid-state electronic devices can be explained based on the quantum and statistical mechanics. The role of quantum mechanics is calculating the carrier-density by introducing the density of states, and filling-factor of the carriers [38]. Beside the role of quantum mechanics in carrier transport calculation, some particular quantum behaviors affect single-photon counter responses [39]. The main quantum effects observed in SPADs include Tunneling phenomena and Bistability/multistability phenomena. The Quantum-dot single-photon detectors (QD-SPDs) are based on a transistor structure in which the conducting channel is close to a layer

of quantum-dots and the resistance of the transistor is sensitive to a change in the occupancy of a single quantum-dot by just a single-electron and so allows the device to perform single-photon detection [40], [41]. It is suggested that by avoiding avalanche process which can amplify both photo-generated carriers and dark-carriers, QD-SPDs offer lower-noise and lower operation-voltage (they are transistor-based so the device can scale with technology and operate at low-voltages [42]). Superconducting Single-Photon Detectors (SSPD) also are nanostructure devices based on long stripes of an ultrathin superconducting film [43] which offer a fast and reliable photon-counters [44] with no leakage-current [42], [45].

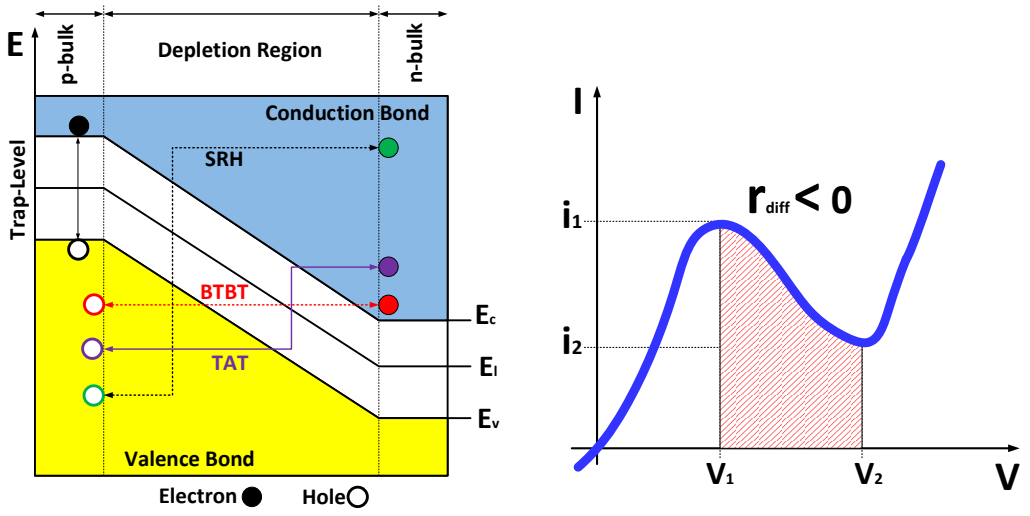
Shockley-Read-Hall (SRH) generation: A free electron thermally excited from the valence -band to the conduction-band can cause an avalanche. However, due to the large and indirect bandgap of silicon, such transitions are extremely rare at normal working temperatures [46]. The traps and defects present in the depletion-region introduce additional energy-levels, acting as intermediate states between the valence and conduction band and thus significantly increase the rate of free-carrier generation. This trap-assisted thermal-carrier generation is known as Shockley-Read-Hall (SRH) process [47]. When SRH generation is the dominant noise source of a SPAD, the DCR doubles every 10°C [42], [46]. The Schottky-barrier photodiodes (SBPDs) are metal-semiconductor photodiodes made by metal-semiconductor hetero-junctions, formed by depositing a thin metal layer (plays the role of n or p layer in the $p-n$ junction) on an n-type semiconductor. This photodetector is responsive to the photon energies larger than the Schottky-barrier height. Due to this low-resistance metal, they offer smaller RC-delay and hence a larger BW [33], [39].

Multiple Excitonic generation: Multiple excitonic generation (MEG) is demonstrated in synthesized nanocrystals (quantum-dots) including PbS, PbSe, PbTe, and Si. MEG is a process whereby multiple electron-hole pairs are generated upon absorption of a single-photon in semiconductor nanocrystals [48]. MEG can be used to increase the solar conversion efficiencies in single-junction photovoltaic cells [49], [50]. In excitonic generation process, electrons and holes in conduction and valence band are generated with different wavelengths [42].

Bistability and multistability phenomena: this effect is mainly caused by defects and traps contributing in trap-assisted SRH-generation, and trap-assisted tunneling. This effect is known as Random Telegraph Signal (RTS) in solid-state electronic devices [42]which is due to the trap-assisted generation or trap-assisted tunneling (TAT). When the charge transport through a solid-

state device it is controlled by changing a trap-state, defect configuration, or a cluster of defects, increases the discrete switching of the current (called burst or popcorn-noise) or RTS [51]. The RTS is important especially for small-area APDs, however reducing the RTSs may increases the flicker (1/f) noise in large-area APDs [42], [52].

Band-to-band and trap-assisted Tunneling: Tunneling (Figure 1.6 (a)) is defined as the penetration of electrons in confined potential barriers can occur between the valence and conduction-band of a reverse biased pn-junction [32]. The tunneling noise is caused by band-to-band and trap-assisted mechanisms [42], and its probability is highly dependent on electric-field magnitude at the pn-junction interface, and the depletion-thickness (junction thickness). Tunneling probability can also greatly increase by the presence of trap energy-levels within the bandgap of the material. The penetration of electrons from the valence band through the depletion region and to the conduction band is considered as one of the main tunneling processes affecting SPADs [46]. Tunneling can contribute to the dark-current in photodetectors and DCR in SPADs in two different processes namely band-to-band (BTBT), and trap assisted tunneling (TAT).



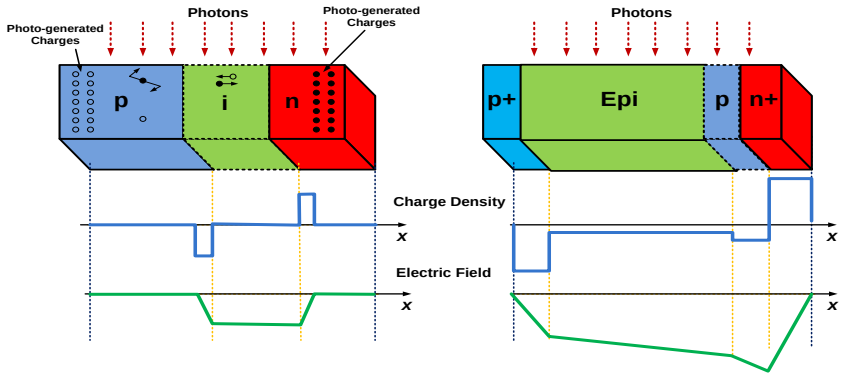
(a) (b)

Figure 1-6: Schematic representation of the Shockley-Read-Hall (SRH) generation, the trap-assisted tunneling (TAT), and the band-to-band tunneling (BTBT) processes (a), and the I-V characteristics of the tunnel diode. It has negative resistance in the shaded voltage region, between v_1 and v_2 (b).

Although BTBT is expected in extreme bias conditions, TAT can occur more frequently. The DCR can be decreased by decreasing the temperature and/or excess bias-voltage. Compared to thermal SRH generation, the tunneling generation rate is less dependent on the temperature [42] and the major temperature dependent DCR contribution is SRH. The TAT is the origin of the stress-induced leakage-current and the resulting gate current increase at low gate-voltage in stressed devices and its probability is strongly dependent on the process-conditions and steps introducing traps and defects [42]. In deep-submicron SPADs, tunneling is particularly high due to the high and shallow doping-profiles and topologies [42], [53]. The tunneling noise can be reduced by using p-well guard-rings or smaller active-area APDs. Increasing the APD active-area, results in higher DCR due to the introduction of more defects and traps [54]. The high-speed tunnel-diode (also called Esaki-diode) has been implemented based on this quantum mechanical effect (tunneling), in which the dopant concentrations in both p and n layers are very high (about 10^{24} - 10^{25} m^{-3}) and so the depletion-layer width is very small to the point where the reverse breakdown voltage becomes zero and the diode conducts in the reverse direction. In forward-bias, this diode operates as a negative-resistance (Figure 1.6(b)) due to the tunnelling which can be applied in solid-state dynatron oscillator, local oscillators for UHF television tuners, trigger circuits in oscilloscopes, high-speed counter circuits, fast pulse-generator circuits, and as low-noise microwave amplifiers [55].

1.2.5 CMOS Silicon Avalanche Photodiodes: Operation Modes

Silicon CMOS avalanche photodiodes (SiAPDs) are more advantageous than photomultiplier tubes (PMTs) which are the most commonly used photodetectors, due to the drawbacks of their vacuum tube technology. Compared to a PIN photodiode, SiAPDs have a bias dependent internal gain which makes them compatible for low-level light detection in the visible and near-infrared (NIR) regions. Accordingly, the photodetector should be highly-sensitive, enabling the reliable conversion of the ultra-low amplitude light signal into a detectable electric signal. SiAPD is a potential candidate for low-level light detection due to its ability to amplify the photogenerated signal by avalanche multiplication. It can be used for realization of high-responsivity and high-speed photodetectors compatible with CMOS technology. The avalanche process can also enhance the gain-bandwidth product with the help of the internal gain effect in avalanche region [56].



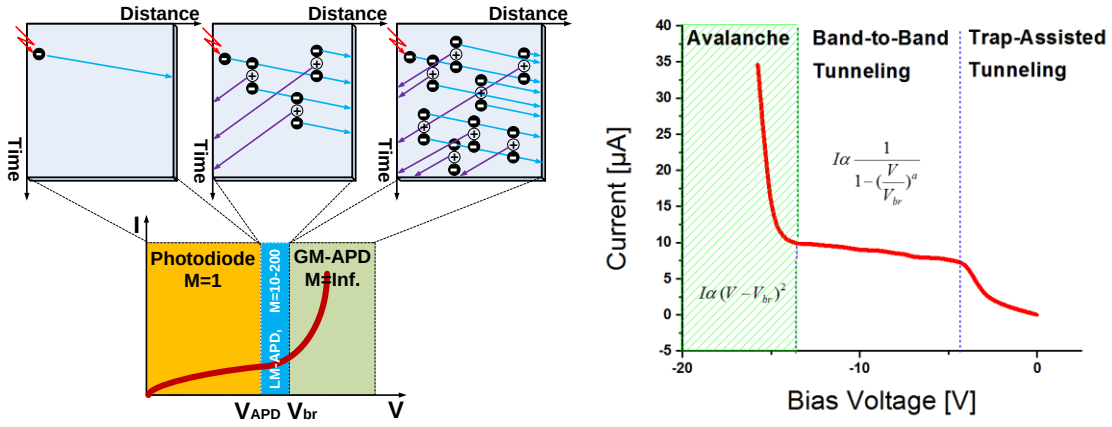
(a) (b)

Figure 1-7: Structure of PIN (a) and Reach-through SiAPD (b) and their charge density and electric field distribution.

Silicon photodetectors fabricated by CMOS process are very promising for short-distance optical access networks and optical interconnect applications [56], [57]. The APD can be considered as a modified PIN junction as depicted in Figure 1.7. The basic structure of an APD contains two regions: photo absorption region and multiplication region. The photon absorption region absorbs incoming photons and converts them to electron-hole pairs. Then the generated primary charge carriers travel to the multiplication region, which is usually formed by a PN or a PIN junction.

When the device is under reverse bias, a depletion region forms across the junction. Due to the space charge, high electrical field develops across the junction. When the primary charge carriers (electrons or holes) enter the multiplication region, they will be accelerated by the electrical field and gain kinetic energy. As the energy becomes high enough, the carriers transfer part of their energy to the lattice and excite new EHPs. Then, the newly generated EHPs will again gain energy from the electrical field and trigger more and more EHPs. As a result, the primary photo generated EHPs are multiplied through the impact ionization process and the internal avalanche gain is produced. When a photon emits to the semiconductor, mobile EHPs can be generated by either band to band transitions (intrinsic excitation) or by transitions involving forbidden-gap energy levels (extrinsic excitation). With well controlled growth processes, band to band transitions are usually the dominant mechanism attributing to the photo absorption process[58]. The light absorption property of a semiconductor is largely determined by the material band structure and especially the band gap energy. In order to excite an electron from the valence band to the conduction band, the incoming photon energy needs to be higher than the band-gap energy

of the semiconductor (λmax (μ*m*) =1.24/*Eg* (*ev*), where *g E* is the bandgap energy of semiconductor). For APDs, internal avalanche gain is generated through the impact ionization process or so called avalanche multiplication process. When a free charge carrier enters the high field multiplication region, with certain probability, it initiates avalanche process, during which the primary carrier can be multiplied. Then at certain point, the ionization chain breaks as the last free carrier exits the multiplication region without exciting subsequent new EHPs due to statistical fluctuation of the impact ionization process. For an avalanche initiated by a single carrier, multiplication gain M is defined as the total number of EHPs generated during the multiplication process. The APDs have a bias dependent internal gain which makes them compatible for low-level light detection in the visible and near-infrared (NIR) regions. The bias of an APD just near but below a breakdown voltage is referred to as a linear-mode operation. At this bias voltage, the gain is high, and the output signal is proportional to the amount of the scintillated light interacting in the APD. The Schematic illustration of Avalanche multiplication and the different sources of the avalanche-current are depicted in Figure 1.8. In linear-mode, only one type of carrier (electron or hole) with higher ionization coefficient takes part in the avalanche process. In Geiger-mode, both electrons and holes produce new electron-hole pairs (EHPs) which take part in avalanche process and promoting a self-sustained avalanche[59],[60],[61].



(a) **(b)**

Figure 1-8: Operation principle of an APD and Avalanche multiplication (a), and the APD current which is originated from trap-assisted tunneling, band-to-band tunneling and avalanche impact ionization processes (b).

While at relatively low voltages in the I-V curve the current is due to trap-assisted tunneling [41], in middle range voltages, the current is due to band-to-band tunneling [62]. Band-to-band tunneling in the reverse current in CMOS technologies is due to very heavy doping (halo) in the vicinity of the source or drain p/n junctions, suppressing short-channel effects by increasing the substrate doping [63].

The tunneling, which describes the transition of carriers through a classically forbidden energy-state, contributes in DCR (or dark-current) using TAT and BTBT processes, so that the total DCR is summation of the DCRs induced by TAT and BTBT ($I_{DCR} = I_{TAT} + I_{BTBT}$). The TAT depends on the generation mechanism of the traps/defects and the process conditions and occurs at low reverse bias voltages. In contrast, the BTBT which is due to the vicinity of the very heavy doped pn junctions, reduces the short-channel effects by increasing the substrate doping [43], and it occurs in higher reverse boas voltages.

The junction-leakage is mainly due to the pocket implants, also called super-halos. This leakage of reversely biased p-n junctions is induced mainly by SRH generation / recombination and TAT at relatively low-voltages and higher temperatures, by BTBT in the middle-voltage range, and finally by impact-ionization avalanche current at high-voltages. The BTBT current around zero bias is usually masked by TAT and SRH recombination currents. So at relatively low bias voltages the APD photocurrent is due to the trap-assisted tunneling (TAT) [41]. However, in middle range reverse bias voltages, the photocurrent is due to the BTBT [26], [62], [64].

In TAT, an electron in the valence-band of semiconductor tunnels across the band-gap to the conduction-band without the assistance of traps and the transition occurs from an initially occupied energy band site to a trapping state with energy (*Et*) followed by tunneling from trap to the final energy-band [38], [40]. The TAT-current (I_{TAT}) is due to carriers that occupy the trap states in the depletion region and tunnel across the junction and depends on the TAT's EHPs generation-rate ($G_{TAT}(z)$) and the probability that each EHP may cause an avalanche ($P_p(z)$) and it can be calculated by an integral over the depletion region as follow [39]:

$$I_{TAT} = S.\int_{z_0}^{z_w} P_p(z).G_{TAT}(z)dz = S.\int_{z_0}^{z_w} P_p(z).\left(\frac{n_i\,.\left(1+\Gamma(z)\right)}{2\tau.\cosh\left(\frac{E_t-E_i}{kT}\right)}\right)dz$$

$$= S.\int_{z_0}^{z_w} P_p(z).\left(\frac{n_i.\left(1+\left(2\sqrt{3\pi}\,.(\xi(z)/\xi_\Gamma).\exp((\xi(z)/\xi_\Gamma)^2)\right)\right)}{2\tau.\cosh\left(\frac{E_t-E_i}{kT}\right)}\right)dz$$

$$= \frac{Aq^2 m_T M^2 N_T U}{8\pi h^3(E_g-E_t)}.\exp\left(\frac{-4\sqrt{2m_T}\,(E_g-E_t)^{3/2}}{3qEh}\right) \quad (1.6)$$

in which, S is the p-n junction interface regions [39], Γ is the field enhancement factor of carriers in each depth of the depletion region, n_i is the intrinsic carrier concentration of the material, τ is the minority carrier lifetime, $E_t - E_i$ is the difference between trap energy and the average energy of valence and conduction bands, k is the Boltzmann's coefficient, and T is the absolute temperature [33], ζ(z) is electric field at each depth of the substrate, q is the charge of an electron, ħ is the Planck's constant, n_i is the intrinsic concentration of material which depends on temperature (T), and band-gap (Eg) [32], N_T is the trap density, m_T is the effective tunneling mass, E_t is the trap energy location measured from the valence band edge and M^2 is the matrix element associated with the trap potential (M^2 for silicon is 1023 $eV^2\ cm^3$ [65]). The TAT of carriers through the ultra-thin oxide-barrier, generates the radiation-induced leakage-current (RILC). In heavily stressed devices, the number of oxide-traps can be considerably high, and the TAT process can involves more than one trap. The generation of vicinal oxide defects, leads to the interaction of the traps in the Stress Induced Leakage Current (SILC) mechanism. In particular, in relatively thick oxides, the presence of only one trap in the oxide can be insufficient to produce considerably large current increases, but the generation of a percolation path due to the presence of several traps can produce very large SILC values and eventually breakdown [25]. The TAT is followed by BTBT in higher reverse-bias voltages due to the higher probability of the band-alignment.

The BTBT-current originates from carriers that tunnel directly from the valence-band to the conduction-band of the pn junction. By assuming a constant built-in electric field across the depletion layer, and a triangular barrier, the BTBT-current (I_{BTBT}) can be calculated based on the BTBT generation-rate ($G_{BTBT}(z)$) and the probability of avalanche creation by each EHP ($P_p(z)$) [66], [32]:

$$I_{BTBT} = S.\int_{z_0}^{z_w} P_p(z).G_{BTBT}(z)dz = S.\int_{z_0}^{z_w} P_p(z).\left(B.|\xi(z)|^{2.5}.D.\exp\left(\frac{-\xi_0}{\xi(z)}\right)\right)dz$$

$$= \frac{Aq^3EU\sqrt{2m_e}}{4\pi^2h^2\sqrt{E_g}}.\exp\left(\frac{-4\sqrt{2m_e}.(E_g)^{3/2}}{3qEh}\right) \quad (1.7)$$

where $B=4.10^{14}cm^{-0.5}V^{-2.5}S^{-1}$, $\zeta_0 = 1.9 \times 10^7 V\,cm^{-1}$ is a constant which depends on the temperature, D is unity except on the edges of depleted-region where it vanishes [39], [67].

In contrast to the I_{BTBT}, the I_{TAT} is proportional to the effective energy difference ($E_g - E_t$), and this makes the I_{BTBT} less sensitive to reverse-bias voltage [65]. Furthermore, the TAT-current is a linear function of the square root of the dielectric field, in contrast to the BTBT-current which is a linear function of the dielectric field. So as it has been shown in Figure 1.8 (b), the I-V plot in BTBT region is relatively flat compared to the TAT region. The BTBT and TAT have been compared more in detail in [68]. It has been concluded that going from large forward-bias (low field-strength) to zero voltage (higher field-strength), first the excess-current due to trap-assisted tunneling is observed, which is then superimposed by BTBT, and finally, the current is determined by BTBT alone. The pre-breakdown range in silicon is dominated by tunneling via traps and in the pre-breakdown range TAT outnumbers BTBT. TAT is described as field-enhanced SRH recombination. The TAT-rate is more than two orders of magnitude larger in the case of the strongly coupled recombination center, and about five orders for the weakly coupled. Only at higher field strengths the BTBT mechanism starts to dominate, due to its steeper dependency on the electric-field [68].

The Geiger-mode APDs (GM-APDs) and SiAPDs (GM-SiAPDs) became of the prominent research topics in the 1960s and 1970s, mainly as a means for replacing the increasingly expensive photomultiplier tube (PMT). The Geiger-mode operation is defined by a bias above breakdown that ensures a signal gain sufficient to count single-photons. It is useful in applications where the photon incident flux is very-low and provides a more reliable and predictable multiplication of signal than a PMT for the same applications. As a GM-APD avalanches in the ON-state, the current through the device increases exponentially. A quenching circuit is used to detect the avalanche-process initiation and reduce the APD bias to suppress the avalanche-current [69]. A reset-circuit is also applied to bring the APD-bias to its initial-state and ready to detect the next photons.

There are a variety of quenching/resetting circuit topologies, and the most common forms include: passive quenching, active quenching, active recharging, and active quenching and recharging[69]. The GM-APDs offered digital-mode operation and compact focal plane arrays (unlike the PMTs) and overcame the high readout noise and subsequently poor SNR of the charge-coupled devices (CCDs) at low-level light (very few photons). As an alternative, the PIN diode can convert a single-photon into a photoelectron, but there is no gain associated with this type of detector (only one signal carrier is generated per photon). Without gain, the electrical signal due to the photon-flux is usually lost in readout noise. For most photon-starved and high-frame-rate applications, the performance of digitized GM-SiAPDs for single-photon counting exceeds the performance of the PMTs, CCDs, and PIN diode detectors[70], [71]. The GM-APDs are well suited to applications involving faint signals and those that would benefit from high frame-rate and accurate single-photon counting capabilities. Such applications include laser-ranging systems, adaptive-optics, astronomy, remote-sensing, and medical imaging.

The avalanche-effect in an APD can theoretically boosts the signal without boosting noise at all, because the only amplification is that of the original photon-generated carrier. In reality, there is an increase in shot-noise (which is a function of the signal flux), and there is some propagation noise in terms of cross-talk. The SiAPDs offer the gain values between 40 and 1000 for linear-mode operation, while materials such as germanium or indium-gallium-arsenide generally only achieve multiplication values of 10-40 [72]. The main characteristics of the Linear (LM-SiAPD) and Geiger (GM-SiAPD) operation modes are shown in Table 1.2 and their Gain-Bias characteristics are compared in Figure 1.9.

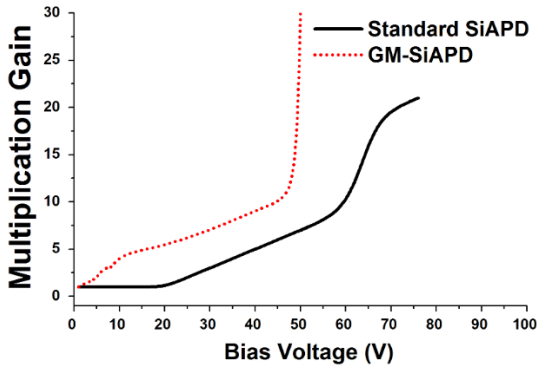


Figure 1-9: Gain vs. Bias Voltage for GM-SiAPD and standard operation APDs

Table 1.2: Performance comparison of the LM-SiAPD and GM-SiAPD

	LM-SiAPD	GM-SiAPD
Pixel Size	Low	High
Device	Amplifier Device	Trigger Device
Noise	Low	High
Speed	Low	High
Electric Power	Higher	Lower
Bias Voltage	Slightly below Vbr	Well above Vbr
Multiplication-Gain	Limited <1000	Unlimited (10k–300k)
Dynamic Range	High	High
Excess noise factor	2	>2
Max. detection probability	25%–100%	<50%
Operating temperature	300°K	240 °K
Voltage bias	Low	High
Detection speed	<1 ns pulses	>20 ns pulses
Afterpulsing	No	Yes
Wavelength	≤2 µm	1–2 µm
EMI* susceptibility	No	No
Reliability	>1000 hr.	<100,000 hr
Crosstalk	No	Poor
CMOS Compatibility	Yes	Yes
Complexity	Low	High

*EMI: Electromagnetic Interference

1.2.6 Infra-Red Detection using CMOS Silicon Avalanche Photodiodes

The Infrared sensors have been available since the 1940s to detect, measure, and image the thermal radiation emitted by all objects [73],[74]. Silicon APD (SiAPD) is a potential candidate for low-level light detection, especially in the visible and near-infrared (NIR) regions due to its bias dependent internal gain and its ability to amplify the photogenerated signal by avalanche multiplication. SiAPDs become popular for several applications including light detection and ranging (LIDAR) [75], military [76], astronomy [77], photon counting [78], and fiber optic communication [79]. They are potential candidate for applications like quantum cryptography [80],[81], profilometry of remote objects [82], fluorescence spectroscopy [83], and biomedical imaging systems such as positron emission tomography (PET) [84], single-photon emission computed tomography (SPECT) [85], and near-infrared spectroscopy (NIRS) [86], [87]. In all of these applications, the applied SiAPD plays a critical rule affecting the overall performance and functionality of the device. The first interface with the human body and the main building block of the fNIRS system is the photo-transceiver front-end. It includes NIR light source(s) and

detector(s). A critical element for NIRS front-end receiver is to design a low-noise and sensitive photodetector to ensure maximum detection of the reflected NIR light that is strongly attenuated by the biological tissues. A minimal signal-to-noise ratio (SNR) of ~40 dB is needed for NIRS application [9]. SiAPDs with dark-current in nA range, and the generated photocurrent in hundreds of μA range confirm SNR of much higher than 40dB. SiAPDs have been commercially available for more than 30 years normally with a dedicated process, which do not allow monolithic integration with other electronic circuitry and no photodetector with aforementioned necessary specifications has been reported, using standard CMOS process, in the literature yet [88].

1.3 Problems studied and previous works

Besides of the significant advantages of fNIRS system it still suffers from some few drawbacks including low spatial-resolution, high-level noise, susceptible to the internal and ambient light/temperature and bias-voltage variations. It is so susceptible to motion artifact that even slight movement (more than 3 mm) will corrupt the image and make it slower to change. Followings are the main studied problems accompanied with the current fNIRS photodetectors:

1.3.1 Bulky systems

As mentioned before, the current commercially available fNIRS devices are not miniaturized enough in order to easily be integrated with other medical imaging systems such as EEG to be used as a wireless and portable device for bedside real-time brain monitoring [89]. So developing a more compact system is required for real-time and portable brain imaging using fNIRS. It will be compact and cost-effective to integrate SiAPDs and other electronic circuits of an NIRS front-end receiver on the same chip using standard CMOS process.

1.3.2 Non-configurability and non-controllability

APD gain and bias voltage affects SNR and therefore error rate of the photodetector [90]. In order to exploit the maximum sensitivity of an APD receiver, it is necessary to bias the APD at a reverse-bias voltage that optimizes the gain for lowest noise equivalent power (NEP) in the presence of solar/thermal background shot-noise, detector shot-noise (due to detector leakage or

dark current), and preamplifier Johnson or thermal noise [91], [92]. Changing the temperature and the reverse bias voltage, and power-supply fluctuation (resulting in low-SNR), changes the detector multiplication gain [93]. Variation of APD gain with temperature could be a serious problem prevents using APDs in some applications [94]. The gain of an APD is a nonlinear function of temperature [95]. The variable and uncontrollable gain of the APD can take it into full avalanche breakdown which can cause catastrophic and irreversible damage to the APD itself [96]. The noise from the APD is also an increasing function of gain so it is desirable to operate the APD such that the gain is just sufficient to bring the shot-noise amplified by the avalanche process to the level of the thermal noise of the preamplifier (this is currently implemented in Hamamatsu APD module C5460-01). Furthermore, the background level variation, changes the optimum value of the gain. So maintaining an optimum gain and bias for operating the APD is a critical challenge in designing any APD-based photodetection system [97], [98]. Several techniques have been proposed for setting the bias of an APD detector [99], [100]. Setting a fixed threshold and provide no optimization for changes in temperature or noise-level, bias-control method using a forward error-correction (FEC) chip and a counter [45], maintain the multiplication factor of APD independent on temperature using extra circuitry (e.g. DC-DC converter, HPF and LPF) [100], APD reverse bias with temperature compensation [101]. In the biasing technique proposed in [102] the APD bias-voltage is controlled by maintaining the APD noise-level constant, but it requires operating synchronously with a transmitted pulse which is subsequently received as a reflection from a target and is not able to control the gain of the APD in the presence of a continuous-wave signal. The proposed method in [103] and [104] uses the information relating to each temperature and the corresponding optimized APD reverse-bias voltage is stored in a memory, then a look-up table has been used to select the proper bias voltage corresponding to the measured temperature. This technique is preferred over the fixed-bias approaches, but does not optimize the gain based on the ambient noise conditions. The technique proposed in [102], [105] ,[92] uses an ambient noise measurement in the bias setting approach. This method considers an APD bias circuit that controls APD gain such that the output noise-level of the APD device matches the preamplifier noise-level with no APD device noise. This approach, however, is complex in its implementation, requires a complicated preamplifier noise measurement circuit, and is not optimum across the range of detector types and anticipated noise conditions [102], [105] ,[92]. A stable gain of the APD can be provided either by thermal

stabilization of the diode unit or by adjusting the reverse voltage. The temperature compensation should keep the APD performance near the best multiplication factor corresponding to the highest SNR. Using a feedback loop to automatically generate an appropriate bias voltage at different temperatures [106], could be a simple solution but its drawback is that the bias is corrected only linearly against the temperature, which is not generally true in usual applications. A CPU-based design has been presented in [107], [108] to keep the APD gain stable under moderate temperature variations. An off-chip active gain-control system for moderate temperature variations is also introduced in [107]. The CMOS CF-TIA with a self-biased automatic gain control (AGC) circuit presented in [109] and [110] also has a high power-consumption (>50mW).

In summary, mainly the proposed control systems for photodetection are based on automatic gain, bias or temperature [111] control. These control blocks are off-chip and/or have been designed in order to control over a limited range of temperature or gain variations [108] and require additional circuitry and techniques for providing thermal stabilization for APD to avoid full breakdown of APDs. Currently there is no integrated real-time control system for simultaneously control of the gain and bias of the APD based on the temperature or other APD photodetector system variations. Furthermore the available photodetection circuitry including amplifier and quench circuits are not tuneable [112] and operate efficiently only on a specific BW, bias, and operating conditions [113]. So designing a new integrated control system for on-chip control and monitoring of the photodetector leads to an efficient and configurable photodetection system which is a serious demand to improve the quality of the currently available non-configurable systems.

1.3.3 Bulky or inefficient photodiodes

Conventional photodetectors use PMTs which are bulky, subtle, sensitive to magnetic-fields and require high-voltage supply. The photodiode used in an fNIRS photodetector front-end requires being highly-sensitive, enabling the reliable conversion of the ultra-low amplitude light signal into a detectable electric signal. Silicon APD (SiAPD) is a potential candidate for low-level light detection in the visible and near-infrared (NIR) regions due to its bias dependent internal gain and its ability to amplify the photogenerated signal by avalanche multiplication. One of the most important topics of research for NIRS front-end receiver is to design a sensitive photodetector to ensure maximum detection of the reflected NIR light strongly attenuated (7-9

orders of magnitude) by the biological tissues. The main design parameters of SiAPD are area, depletion region thickness, SNR and fabrication technology and architecture. High-level noise and low-efficiency of the currently available detectors [114], [115], encouraged us to design a new CMOS SiAPD with low-noise and high efficiency characteristics at NIR region.

The SiAPD fabrication in dedicated CMOS process suffers from two major disadvantages: the production cost is very high due to the specialized fabrication process, and it is impossible to integrate it with the electronic circuits on the same chip. Optimizing the performance of both the CMOS devices and the SiAPD is a non-trivial job. To overcome these problems, researchers have investigated the design and fabrication of SiAPDs using standard CMOS process [115], [116]. The advantages of standard CMOS fabrication process are: the availability of a fully supported, mature and reliable technology at reasonably low-cost, and the possibility of developing a complete system on chip with a high-degree of complexity. The mandatory requirement for SiAPD fabrication in standard CMOS process is that a suitable subset of CMOS fabrication process-flow should be able to build a planar p-n junction without device breakdown at the photodiode periphery. SiAPDs fabricated using standard CMOS process involves high-doped p or n layer resulting in shallow or medium depth depletion region. As a consequence, the fabricated SiAPDs using standard CMOS technology, usually are inefficient to detect red and NIR photons, and are not suitable for NIR signal detection in neuroimaging. However, to increase the use of SiAPD-based front-end receivers for biomedical applications, integration of the SiAPD and peripheral circuitry on the same chip using standard CMOS technology is highly desired. The fabrication of SiAPDs in standard CMOS technology permits fabrication of both the photodetector and the necessary peripheral circuits on the same chip for an integrated system. However, it is challenging to make SiAPDs in CMOS technology due to lack of special fabrication steps. Several research groups have fabricated SiAPDs using standard CMOS technology. The area and design of the SiAPDs for different CMOS technologies are different which results in a wide range of performance matrix of SiAPD. Photon-detection efficiency is better for larger area SiAPDs. SiAPDs with larger area can more suitably be designed using older CMOS technology. However, use of older CMOS technology will increase area and power-consumption for the rest of the electronic circuits of the NIRS front-end receiver. On the other hand, doping concentration levels in CMOS increase as the technology advances, causing an increase in the peak electric field in the depletion region and decrease in the breakdown voltage

of the diodes. Advanced CMOS technology offers SiAPDs with low breakdown-voltage ensuring safer operating condition for biomedical applications. The amount of reflected NIR light photons detected by the photodetector depends on the power of the NIR light source, the attenuation due to biological tissue, and the light source-to-photodetector distance. The level of attenuation with a light source-to-photodetector distance of 4 cm, for a five-layer (scalp, skull, cerebrospinal fluid (CSF) layer, and gray and white matters) head model, can be approximated by 4.12 $\times 10^{-4}/cm^2$ [114]. Thus, the area of the photodetector should be large enough so that it can capture enough optical photon to generate detectable electric signal. Earlier silicon PIN photodiodes were successfully used for NIRS systems with an active area of ~7.5 mm^2 [114]. SiAPDs are also commercially available with comparable active-area and are being used in several NIRS systems, such as, Hamamatsu C5460-01 device which has a large active-area of 7 mm^2. However, these commercial SiAPDs necessitate a dedicated fabrication process, and cannot be fabricated on the same chip with the rest of the NIRS device. As such, fibre-optic bundles are used to guide the NIR light photons from the scalp to the photodetector which results in loss (up to 40%) of optical signal. On the other hand, the performance of SiAPDs fabricated using standard CMOS process degrades with increase of its area which limits its active-area to 0.003 mm^2. Recent advancements in the standard CMOS fabrication process allow producing SiAPDs of active area up to 0.3 mm^2 (~200 µm diameter) while maintaining excellent performance. The higher the thickness of depletion-region of SiAPD, the better is its photon absorption efficiency. However, a thick depletion region increases the noise of the SiAPD. To ensure a reasonable amount of photon-absorption (~70%) in NIR range, it is of primary importance to design SiAPDs with at least 10 µm thick depletion region.

1.3.4 Inefficient photoreceiver and amplifier

Based on the mode of operation, we need different kinds of amplifiers and processing blocks after photodetector. For linear-mode operation, SiAPD requires a transimpedance amplifier (TIA) to convert the input photocurrent into a voltage signal. Due to the low-level and usually high source-impedance of fNIRS signals, this amplifier should be established to meet certain basic requirements and must cope with various challenges. The main challenges of designing such a TIA for portable biopotential acquisition systems are: High Common-Mode Rejection-Ratio (CMRR) to reject the interference from the mains, High-Pass Filter (HPF) characteristics for

filtering differential DC offset, Low-noise for high-signal quality, low power-dissipation (<50mW) for long-term power-autonomy, configurable gain and filter characteristics that suit the needs of different biopotential signals and different applications, high transimpedance-gain (>1k), narrow-Bandwidth (around 100 kHz), high output-swing, wide dynamic-range, ambient-light rejection, and low-voltage operation. However, designing such a proper dedicated front-end for fNIRS has not been considered in the literature yet and none of the reported NIRS detectors provides these features taken together, which is a crucial factor in real-time brain imaging.

Available proposed amplifiers for this case [117], [118] are suffering from a lot of limitations so that trade-off between necessary parameters occurs with the cost of losing reliability and performance. For example reported variable-gain transimpedance amplifiers are difficult to stabilize. The key problem with these designs is that they are based on the traditional two-stage topology consisting of a common-source gain stage followed by an output buffer. Phang et al. [119], [120] proposed a TIA combining a sub 1-V current mirror [121], [122] and a common-gate TIA [122] based on a current-gain amplifier for optical communication. Achigui et al. [117] modified this TIA by adding an OTA with dynamic-threshold transistor (DTMOS) for NIRS front-end photoreceiver. All of these designs are based on a fixed-gain and only one mode of operation. Reaching high data-rate and high-BW in these designs is also with the cost of small gain, high noise and power-consumption. So the needs for a new design with the ability to overcome these limitations and cover the requirements for a fNIRS photodetector front-end, is a critical issue which this research has addressed. There are mainly three TIA structures reported in the literature: common-gate TIA, resistive feedback TIA, and capacitive feedback TIA. Common-gate TIA(CG-TIA) [123], usually used in open-loop topology and exhibits low input-impedance and high transimpedance-gain, however its input current-noise and input bias-current are high and its BW is also low. In resistive-feedback TIA(RF-TIA) [124], the transimpedance gain is high and offers the smallest noise specially at high frequencies comparing to other structures, but its BW is limited. Capacitive-feedback TIA (CF-TIA) [110], offers lower noise at low frequencies but it is noisy at higher frequencies. A common-gate configuration is typically chosen as it can tolerate a wide range of SiAPD capacitance. However, resistive feedback architecture has better noise performance and is more attractive when SiAPD models are readily available.

1.3.5 Slow quench-reset systems

In Geiger-mode, SiAPDs work as trigger devices rather than amplifying devices. For operating the SiAPD in Geiger-mode (single-photon counting mode), the quenching and reset circuits are necessary. Unlike linear-mode SiAPDs, silicon single-photon APDs (SPADs) are not concerned with gain fluctuations since here the gain is virtually infinite. Additionally, in Geiger-mode, the signal amplitude does not provide intensity information since all the current pulses have the same amplitude. Intensity information is obtained by counting the pulses during a certain time frame or by measuring the average time interval between successive pulses. Generally three types of quenching circuits have been used for Geiger mode operation: passive, active and mixed quenching circuits. Passive quenching (PQ) or self-quenching is the first and simple method of quenching an avalanche was employed since the early studies on avalanche breakdown in p–n junctions by Haitz [125]. All later quenching circuits were developed starting with the principle of this one. It has two possible configurations: voltage-mode output and current-mode output. The voltage-mode provides longer pulses, which might be convenient to visualize them in the oscilloscope but might hinder high-speed detection and the detector timing performance is not fully exploited. On the other hand, the current-mode output configuration allows high detection-rates. PQ is suitable for SPADs having small RC time-contacts since it can be operated at higher speed. PQ circuit is an easy to implement and an effective method of quenching for small area (less than 50μm) devices since they have very low capacitance (capacitance scales with area) and hence higher-speeds is possible with PQ. They can also be used with large-area devices where high counting-rate is not a requirement (~few hundred kHz). Since, the selected SPAD for our application is a large area device that is expected to count photons at high-speed (≥ 1MHz), PQ is not a feasible option.

In order to achieve faster quenching, active quenching circuit (AQC) is used. This method forces back on the SPAD to drop the bias-voltage much quicker enabling significant speed improvements over the PQ method. It causes high-accuracy in photon-timing. Small-delay in quenching the avalanche resulting in fewer carriers crossing the junction and hence lower false re-triggering of avalanche (lower after-pulse). This also results in lower power-loss and hence less-heating of the SPAD. The Dead-time of the circuit does not depend on the component values and can be accurately controlled, hence precise determination of the dead-time is possible for satisfactory circuit operation. The concept of AQC, was introduced for the first time in [126] and

applied for photon-timing in [127]. Once the quenching action is initiated, the high-voltage pulse must be applied as soon as possible to minimize heating and after-pulsing effects. A timing-circuit controls the dead-time of the AQC. The dead-time is composed of two different parts, the quench-time and the reset-time. During quench-time, the SPAD bias is held below breakdown and reset time allows the SPAD to recharge back to the actual bias voltage. However, it is difficult to design an effective AQC and it needs extra and complicated ultra-precise circuitry to reduce the propagation-delays as well as stray-capacitances [111]. So, even though the AQC is a fast method for quenching the avalanche comparing to PQ, it is not the most preferred method.

1.3.6 Low depth and spatial resolution

Spatial-resolution of NIRS is not sufficient to distinguish between motor and sensory activation in neuroimaging studies [128]. The amount of reflected NIR light photons detected by the photodetector depends on the power of the NIR light source, the attenuation due to biological tissue, and the light source-to-photodetector distance [129]. To obtain information about optical properties of thick tissue, the scattering and absorption coefficients at different wavelengths must be determined. Unfortunately, the effects of scattering and absorption cannot be distinguished in simple steady-state images. We can directly detect the light diffusion through the tissue using pulsed light transillumination to discriminate the scattering and absorption and improve the depth resolution with cost of low-SNR. Stronger scattering and absorption, both decrease the output intensity, but stronger scattering increases the pulse width while stronger absorption decrease it.

In the photon migration literature the use of short source-detector distance (SDD) in the time-domain (TD) has always been avoided with the aim to fulfill the requirements of photon diffusion theory at all times. NIR photons carry very little information when collected at small distances [130]. Further apart the source-detector, the deeper the photons reach inside the tissue. The source-detector separation is limited by the SNR of system, such that the light intensity decreases exponentially with the distance from the source. Several SDDs in the range of zero to 6cm, has been proposed in literatures for different applications. Although for CW the depth sensitivity is larger for greater SDD, but in TD the depth sensitivity can be improved by exploiting the temporal information. The most severe obstacle to null source-detector separation (NSDS) is the presence of early-photons. An efficient mechanism to gate, or at least to considerably reduce, the early-photons, leads to exploit the advantages of time-resolved reflectance at null source-detector

distance (NSDD). By means of time-gating in TCSPC it is possible to detect longer lived photons neglecting initial ones. Exploiting the information content encoded in the late diffuse photons, while disregarding the early, weakly diffusive photons. NSDS idea originally proposed by Bianco et al. [131] and developed by Torricelli et al. [132]. This technique, improves the depth and depth-sensitivity of the current counters. Working in NSDD, causes the increased number of collected photons at any time, contrast, spatial-resolution, and simplified measurement geometry with potential advantages for reconstruction. Time-domain(TD) systems can provide better depth-sensitivity than CW systems, by gating late photons which carry information about deep layers and rejecting the early-light sensitive to the superficial signal clutter, but they are bulky, need complicated extra circuitry and are relatively expensive [133].

1.3.7 Noise problems

The noise included in fNIRS is an important limitation. The movement, heart-rate, breathing-rate, and low-frequency oscillations can affect the NIR signal. Head movement can cause the NIR detectors to shift and lose contact with the skin, exposing them to either ambient light or to light emitted directly from the NIR source or reflected from the skin, rather than being reflected from tissue in regions of interest. SiAPDs offer substantial advantages over normal photodiodes since the SNR of SiAPD for low-level signal is determined by thermal or amplifier noise and not by the shot-noise in the photodiode current. In linear (proportional) -mode of SiAPD, the statistical variations of the finite multiplication gain also produce a noise contribution known as excess-noise preventing linear SiAPDs from single-photon detection. Although, the thermal noise is not a limiting factor on APD performance, but due to the internal gain mechanism of APD, its performance is limited by the shot-noise due to the detected signal, background signals or the detector leakage current. Since avalanche multiplication is caused by carrier impact ionization events which occur with statistically distributed probability, it is intrinsically noisy. As such, the performance of SiAPD is degraded by a factor known as excess-noise factor. Both excess-noise and photocurrent of SiAPD increase as the avalanche gain increase, so the best SNR occurs at a certain gain. A SNR of ~40 dB is needed for NIRS application [9]. SiAPDs with dark-current in nA range, and the generated photocurrent in hundreds of μA range confirms SNR of much higher than 40 dB. But a photodetector with these necessary specifications has not been reported in the literature yet.

Gated photon-counting (GPC) [134] is very useful for recording the intensity of a high-repetition rate pulsed signal in a fixed-time window defined by a gate-pulse triggered externally (e.g. by a photodiode receiving the pulses of the excitation LED(s)). Using GPC we can suppress the background counts from the detector in the time intervals where no signal is present. It is also able to separate the fast and slow effects, e.g. Raman scattering and fluorescence or fluorescence and phosphorescence [134]. GPC can suppress the background and detector gain noises, improves the time-resolution, and its sensitivity is independent of detector gain variations over a wide range. It includes a discriminator that has an adjustable threshold, which is set to discriminate the single-photon pulses against the background noise [134]. By exceeding a single-photon pulse from the threshold, the discriminator produce a pulse with a specific level and duration. Although the GPC measures the intensity, it also can be used in order to record the waveform of repetitive light signals by running a large number of measurement cycles and sampling the waveform of the input signal by scanning the delay of the gate-pulse [134]. Using GPC improves the time-resolution, baseline stability, and SNR. However, its efficiency is low because of the rejection the large part of the detected photons by a narrow gate. In order to improve the efficiency of the GPC, the multi-gate photon counting (MGPC) can be applied which yields a counting efficiency close to one [134]. In this method the detector photon pulses counted directly using several parallel gated counters. The gates are controlled using separate gate-delays and by separate gate-pulse generators. MGPC was developed primarily to obtain fluorescence life-time data within short acquisition times by conquer the count-rate limitations of the TCSPC devices.

1.4 Conclusion

Functional near infra-red spectroscopy is a new noninvasive technique with a potential to be applied for long-term portable brain imaging applications. However, this potential has not been quite realized yet due to bulky and high-voltage components to develop the photodetector front-end of this system. Towards finding a solution for aforementioned problems, here we have composed several questions which are listed bellow:

- Is it possible to further miniaturize the currently available fNIRS photodetectors for portable and real-time monitoring of brain?
- How to design a CMOS photodiode with high detection-efficiency and low-noise?

- How to design an integrated low-noise, high-gain and low-power photodetector amplifier for fNIRS imaging?
- How to design a configurable photodetector front-end to overcome the speed, noise and power-consumption limitations?

Next chapter explains the research method applied in this thesis for answering these questions.

CHAPTER 2 RESEARCH METHODOLOGY AND ORGANIZATION

This chapter concerns the research objectives and the outline of applied reserach methods towards reaching the specific objectives of the study.

2.1 Purpose of the Study: Objectives and Hypothesis

The general objective of this research is to develop a new miniaturized, reconfigurable, low-power, low-noise and high-gain fNIRS photoreceiver for real-time brain imaging. The specific objectives and hypothesis include:

(a) Miniaturizing the currently available fNIRS photodetectors for portable and real-time monitoring of brain.

Hypothesis: Using CMOS image sensor concept for fabrication of photodiode and photodetection circuitry and integrating them on the same chip with ability to works on different modes of operations, leads to a more compact and miniaturized design.

Originality: Integrating the photodiode and photodetection circuitry on the same chip and on-chip multi-mode operation using CMOS image sensor concept has not been considered yet in literature for fNIRS application.

(b) Design a CMOS photodiode with high detection efficiency and low-noise.

Hypothesis: Using p+/n-well topology, with guard-ring and negative feedback avalanche concept in fabrication of CMOS photodiode, increases the efficiency and reduces the noise level.

Originality: This is the first application of negative feedback avalanche in p+/n-well silicon CMOS avalanche photodiode with guard-ring topology and no similar implementation has been reported yet.

(c) Design an integrated low-noise, high-gain and low-power photodetector amplifier for fNIRS imaging.

Hypothesis: Combination of Common-Gate (CG) and Resistive-Feedback (RF) -TIA topologies based on DTMOS, and using logarithmic-TIA (LogTIA) and distributed-gain concept leads to a configurable low-power, low-noise and high-gain TIA front-end.

Originality: Designing a dedicated TIA by combination of DTMOS CG and RF-TIA is not considered yet in the literature. This is the first application of LogTIA and/or distributed-gain concept in fNIRS front-end.

(d) Design a configurable, fast, low-noise and low-power photodetector

Hypothesis: Integrating the photoreceiver with adaptive-optimal control system using CMOS smart image sensor technology leads to a configurable, low-noise, low-power, high-gain and fast photodetector to be applied real-time for brain imaging.

Originality: Real-time on-chip monitoring and multi-model adaptive-optimal control of fNIRS photodetector regarding to its optimal gain, bias, temperature and noise is a novel idea hasn't been used in any similar photodetector yet and this is the first proposed integrated adaptive-optimal control system for smart image sensor to be used for fNIRS photodetection.

(e) On-chip integration of APD with CW/Photon-counter circuitry.

Hypothesis: On-chip integration of the photodetector and the CW/Photon-counter circuitry, improves the efficiency and speed, and leads to a miniaturized, low-noise and low-power fNIRS photodetector.

Originality: On-chip implementation of the SiAPD and processing circuitries has not been already implemented in fNIRS front-ends.

2.2 Proposed Work and Methodology

A new fNIRS photoreceiver front-end is introduced to be used in a wireless real-time brain imaging system. The overal block diagram of the proposed photoreceiver is depicted in Fig. 2-1. The main focus of this thesis is only on design and implementation of the APD, the circuitry for CW-fNIRS (include TIA and filter blocks), and the photon-counter circuitry (include Quench-Reset and control blocks). Implementing a low-power/low-noise APD with peak photon-detection efficiency in NIR region of light spectrum and its integration with introduced CW and photon-counting circuitries, have been also addressed in this thesis.

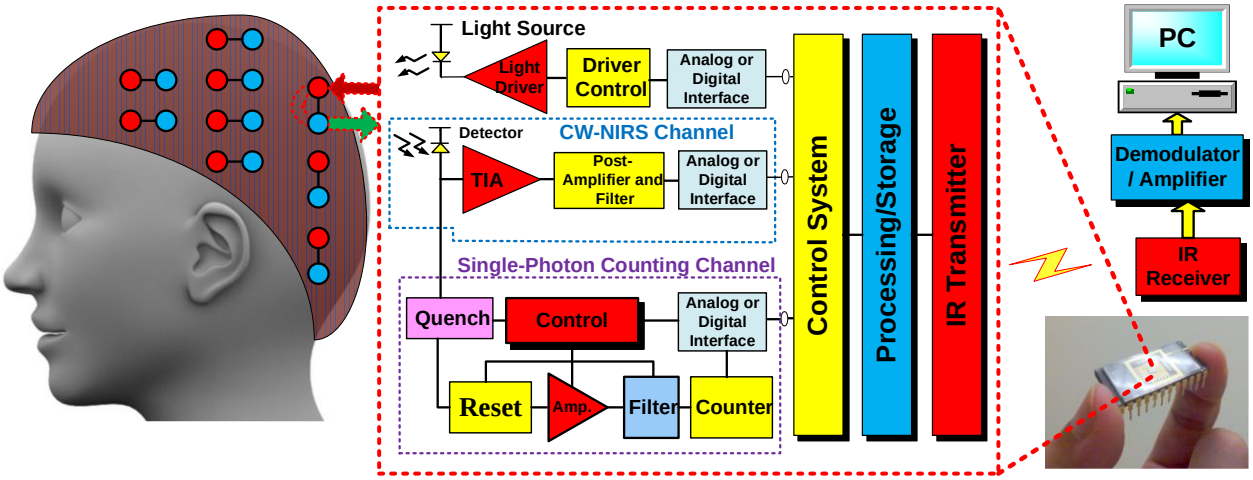


Figure 2-1: Block diagram of the proposed integrated CW/TR fNIRS for real-time Brain Imaging.

2.3 Methodology

In order to achieve the above described objectives, based on the original scientific hypotheses of the contribution we have proceeded as follows:

2.3.1 Design and implementation of a CMOS avalanche photodiode

We have used standard CMOS technology to implement a SiAPD for NIR light detection. Using standard CMOS technology permits fabrication of both the SiAPD and the necessary peripheral circuits on the same chip for an integrated system. However, it is challenging to make SiAPDs using standard CMOS technology due to the technology design-rules restrictions and lack of special fabrication steps. We have used 0.18µm and 0.35µm CMOS technologies, device simulators, CADENCE schematic editor and Virtuoso layout editor in order to achieve optimal design, simulation and implementation of the SiAPD.

2.3.2 Designing an integrated circuit for operating in both Linear and Geiger modes of operation

In order to properly bias and utilize SiAPDs in practice, several peripheral circuitries have to be used based on the application and mode of operation. One of the main advantages of using standard CMOS technology is ability to integrate the SiAPD with these peripheral circuitries.

Several circuitries have been developed to be integrated with APD for bias, filtering and noise reduction, amplification, control and tuning, and signal processing. These circuits can be divided in two distinct categories based on the APD mode of operation: Linear (LM-SiAPD) and Geiger (GM-SiAPD).

Linear-mode circuit design: In LM-SiAPD, the APD if followed by a TIA. For linear-mode of operation we have designed a transimpedance amplifier (TIA) at this stage to convert the input photocurrent into a voltage signal. Here we have introduced three new TIAs. However some other components also have been added to amplify, filters and enhance the process but in general the linear-mode circuitry can be simply a TIA.

Geiger-mode circuit design: In order to operate the single-photon avalanche photodiode (SPAD) in Geiger-mode for single photon-counting, a quenching-circuit and a reset-circuit have been designed in this stage. We have designed a new, fast, low-noise and high-efficient quench-reset circuit by combination of the previously applied active and passive techniques in this stage to be used along with the photodiode in Geiger-mode for high-speed single-photon counting. In order to make the avalanche quenching as fast as possible, we have also introduced a new hybrid approach using a controllable mixed-quenching circuit (CMQC).

2.3.3 Integrate a complete one-channel photoreceiver circuit

We have applied CMOS technology to design and fabrication of the integrated circuit for fNIRS photoreceiver front-end. The implemented APDs have been integrated with photodetection circuitry and control system towards offering a single-channel on-chip photoreceiver front-end.

2.4 Summary of Contributions and Outcomes

The complete list of the publications based on this work are shown in Appendix 1. The main contributions of this thesis are listed below:

2.4.1 New SiAPDs in 0.35 µm and 0.18 µm CMOS technologies

New SiAPDs have been implemented using standard 0.35µm and 0.18µm CMOS technologies.

Impact of device simulation and its role in an efficient SiAPD fabrication are addressed based on our design, simulation and fabrication experiences. The effects of premature edge breakdown (PEB) and available PEB prevention (PEBP) techniques in silicon avalanche photodiode fabrication using the standard CMOS process have been scrutinized. The most common PEBP techniques are implemented following by a systematic study aimed at miniaturization, while optimizing the overall performance. By implementing different SiAPD structures, we studied the geometric trade-offs involved in the design of deep-submicron SiAPDs.

The p-well-, p-sub- and n-well-based PEBP techniques are evaluated and compared based on simulation and fabrication results using the standard CMOS process. The results demonstrate that the n-well guard ring offers the most efficient PEBP technique. The p-well and p-substrate structures suffer from punch-through, high tunneling and PEB. However, the SiAPD with the n-well-based guard-ring structure offers the highest sensitivity and PDP-to-DCR ratio characteristics and could be biased properly in the Geiger-mode. This technique offers a high-gain (~800), low-noise dark count-rate (DCR = 40 Hz), high detection-efficiency (70%) avalanche photodiode with a higher functionality probability.

A new PEBP technique has been introduced based on the APD-Shaping. Using this technique (called Shaping-PEBP) by implementing APDs in Rectangular, Octagonal, Hybrid-Octagonal, Netted (Reticulated), Nested (Maze-Shape), Quadratic, and Hexadecagonal shapes have improved the APDs characteristics with a more efficient PEB prevention. Using shaping-PEBP (SPEBP) technique has increased the functionality and offered ADPs with higher-PDE and less-noise compared to the conventional PEPB techniques.

2.4.2 New integrated circuits for CW-fNIRS

Three new Transimpedance amplifiers have been introduced and implemented using standard CMOS technology.

The first introduced TIA has been designed using distributed-gain concept combined with resistive-feedback and common-gate topology and offers a transimpedance-gain up to 250 MV/A, tunable-BW (1 kHz – 1 GHz), input and output noises of 100 fA/√Hz, and 1.8 μV/√Hz, 0.8 mW power-consumption, with stability (phase-margin ≥ 40°), and robustness against power-

supply variation (1V– 3V). This implemented TIA also shows efficiency in different bias voltages.

The second TIA is a distributed-gain 4-stage amplifier, targeted towards offering high-GBW. This TIA offers a 4mW power-consumption, a transimpedance-gain up to 250MV/A, tunable BW in a wide-range (100KHz-1MHz) and low-input and output noise (280fA/√Hz and 1.5mV/√Hz) characteristics.

A new Logarithmic TIA (LogTIA) with automatic gain control (AGC) and ambient-light rejection is also introduced for low-level light detection applications. This TIA has been implemented in 2 different CMOS technologies. Using AGC and noise-rejection in LogTIA have reduced the input-current noise (with factor of 0.1) and have increased the GBW (with factor of 6.8) compare to the regular LogTIA.

2.4.3 New integrated circuit for TR-fNIRS: Photon-Counting

In order to operate the SiAPD in Geiger-mode for single-photon counting, a new high-speed, low-power and controllable photon-counting technique is introduced and implemented using standard CMOS technology. It includes an integrated hold-off time control and on-chip counter in a small-area which offers a quench-time smaller than 10ns with a 0.6mW power-consumption and less-complexity accompanied with more flexibility and dynamic-range of operation by developing an adaptive and fast hold-off time control on the available traditional quench circuits. Decreasing the avalanche time duration has reduced the power-dissipation, charge-trapping and the optical crosstalk noise. Characterizing the proposed device in response to single and multiple photon detections show its preference specially regarding to the power-consumption, speed, controllability and scale (FF).

2.4.4 On-chip integration of APD with CW and Photon-counting circuits

The main effects of on-chip integration on the performance and efficiency of silicon avalanche photodiode (SiAPD) and photodetector front-end have been addressed in this thesis based on the simulation and fabrication experiments. The on-chip integrated SiAPDs show higher signal-to-

noise ratio (SNR), sensitivity and detection efficiency comparing to the separate SiAPDs. The integration does not show a significant effect on the gain and preserves the low power-consumption. Using APDs with p-well guard-ring is preferred due to the higher observed efficiency after integration.

The on-chip integrated APDs with the TIA preserves the high-performance characteristics of both APDs and TIA while offering a more miniaturized photodetector front-end dedicated to low-level light detection applications. The integration improves the SNR, sensitivity, fill-factor (FF) and photodetector frequency-response (PFR) with no significant change in power and gain values. Using APDs with larger active areas and applying p-well guard-ring is also preferred due to the higher observed efficiency after integration.

We have also shown that on-chip integration of the APD and photon-counting circuitry, in additional to offering a higher fill-factor designe, reduces the after-pulsing and increases the sensitivity accompanied with a significant decrease in power-consumption. The on-chip integration has increased the SNR in additional to offering a faster response (2-5 ns) compared to the non-integrated APD and photon-counter.

2.5 Thesis Organization

This is a paper-based thesis and it is presented in 6 chapters and 4 appendices as follow:

Chapter 1: Introduction and theory background

This chapter covers the theoretical background, critical literature review and stating the problems accompanying with the motivations of the research.

Chapter 2: Research methodology

This chapter explains the objectives and the applied methods towards reaching the research goals, followed by the list of the contributions.

Chapter 3: SiAPD design and implementation

The implemented SiAPDs characteristics and their design challenges (design and fabrication of the SiAPDs using Standard CMOS Technology) are explained in this chapter and Appendix 2 (JSST Paper). The impact of the premature edge-breakdown (PEB) and characteristics of the

implemented SiAPDs using p-well, p-sub, and n-well guard-rings have been covered in detail in Appendix 2.

Chapter 4: SiAPD front-end circuitry for CW-fNIRS Photodetection

The design and implementation of the front-end circuitries for CW-fNIRS are explained in this Chapter (Design and implementation of the TIA) and Appendix 3 (IEEE Sensors Paper). The implemented distributed-gain TIA (TIA1) and the impact of the on-chip TIA+APD integration have been reported in Appendix 3.

Chapter 5: SiAPD front-end circuitry for TR-fNIRS Photodetection

The proposed circuits and system for time-resolved fNIRS and photon-counting are introduced in Chapter 5 and Appendix 4 (TBioCAS Paper). The implemented mixed-quench (MQC) and Controllable MQC (CMQC) circuits and the impact of on-chip integration of APD with photon-counter circuit have been explained in Appendix 4.

Chapter 6: Conclusion and future work

The Conclusions and Future Works are introduced in Chapter 6.

Appendices

The thesis is in paper-based format. So that the papers are placed in the appendixes and the content of the thesis explains the research background, methodology and achievements.

CHAPTER 3 CMOS SILICON AVALANCHE PHOTODIODES: DESIGN AND FABRICATION

3.1 Introduction

Silicon-based semiconductors offer excellent thermal and mechanical stability and are pushing the industry to an ever-increasing level of integration. However due to the indirect bandgap of silicon that makes it not to be a strong light emitter, the III-V semiconductors are mostly used in the photonic industry [1], [135]. Silicon-based avalanche photodetectors can be applied as an efficient, low-power, compact, safe, cheap and sensitive tool for near infra-red light detection. Using proficient techniques to implement these photodetectors in standard CMOS process will launch more their confidence to be applied in different fields of science and technology. Overcoming some difficulties related to their skilful and practised fabrication using standard CMOS process, offers miniaturized, reconfigurable and low-noise light detectors which can be designed especially for high-sensitivity in NIR region of light spectrum.

3.2 Design Challenges of Near Infra-Red Detectors

The quality metrics to design a high-performance image sensor for low-level light detection, depend on both the pixel architecture and the photosensitive structure. Several parameters of photosensing using junction diodes such as photocurrent, dark-current, junction capacitance, breakdown voltage, thermal noise and shot noise depend on the avalanche photodiode (APD) structure and type of the junction. In addition to the junction characteristics, the location of the junction also contributes to spectral sensitivity. In particular, two main manufacturing processes for APD fabrication can be distinguished:

a. Dedicated technologies, which improve performances by optimizing individual technological parameters. They generate low-noise high-quantum-efficiency sensors via thick depletion layers (> 30μm), but integration of electronics with sensor is impossible. SiAPDs fabricated using highly-optimized dedicated processes offer an excellent device performance, because they can have low-doped p and n layer resulting in wide depletion-region extending from the cathode to the anode. Due to the availability of wide depletion region, they are efficient for absorption of red and NIR photons. Nevertheless, the SiAPDs fabricated in dedicated process have two major

disadvantages: the production cost is very high due to the specialized fabrication process, and it is impossible to integrate electronic circuits on the same chip. Later several dedicated SiAPD fabrication technologies were proposed[136],[137],[138] which are compatible with the fabrication of CMOS circuits, and therefore, monolithic integration of APD devices and CMOS circuits became possible. However, optimizing the performance of both the CMOS devices and the SiAPD is a non-trivial job. The investigation of other industrial CMOS processes is one possible way to fabricate larger APDs with enhanced detection probability in the red/IR spectral range. Different techniques should be studied such as back-side illumination, SOI, and SiGe technologies in order to improve the APD performance.

b. Standard CMOS processes or CMOS compatible technology. To overcome the problems of dedicated CMOS process, researchers have investigated the design and fabrication of SiAPDs in a standard CMOS process to reduce the cost and to maximize the miniaturization[9],[139]. The fabrication of SiAPDs in standard CMOS technology permits having both the photodetector and the necessary peripheral circuits on the same chip as an integrated system. However, it is challenging to make SiAPDs in standard CMOS technology due to lack of special fabrication steps. Fabrication of APDs using standard CMOS process facing several significant challenges, making it one of the most difficult and non trivial areas in semiconductors design and implementation. In standard CMOS technology, it is impossible to separate the photon absorption-region and the multiplication-region of the carriers, due to the realization of the multiplication in a very thin absorption-region where the electric-field is maximum.

One of the main difficulties for optimal CMOS APD design and fabrication is the technological constraints imposed by CMOS chip manufactures (e.g. AMS, IBM and TSMC). Manufactures do not give out doping profile information for their technologies, and do not allow to the designer to make any modification on the normally available layers. Referring to the applied technology layers doping and depth characteristics, we can point out the weak depths and the high doping values applied in the technology (For example Table 3.3 and 3.4 show the main characteristics for CMOS 0.35-μm and 0.18-μm technologies).

3.3 Premature Edge-Breakdown (PEB) Effects

The realization of the APD has to be compatible with the CMOS process characteristics and the APD has to operate with a sufficient voltage, allowing for avalanche mode without destroying the device, particularly at the peripheral junction at the presence of Punch-through, high tunneling, and premature edge breakdown (PEB) effects[140]. The punch-through effect (which observed frequently where the n-wells could not join each other) is due to this fact that the doping-profiles and distances between junctions cause that the depletion regions of two superimposed layers touch, thus causing an ohmic resistance that effectively short-circuits cathode and anode[42]. Due to elevated doping-profiles also, tunneling dominates thus preventing the control over dark count rate (DCR) and causing the APD to operating as a Zener diode.

CMOS SiAPDs work in avalanche mode which necessitates application of high-voltage across the device. As such, there is a risk of premature breakdown of the device, particularly at the junction peripheral edges since higher electric field exists at the periphery. This is called premature edge breakdown (PEB). In this case, most of the charge multiplication events will be triggered by thermal generation, which gives rise to large values of dark-count and would prevent the light detection in APD. The PEB affects on the functionality of APD in Geiger-mode (more details have been explained in Appendix 2). However a circular shape is desired for APDs to reduce the possibility of corner breakdown, it might not be implantable in standard CMOS technologies because the layout rules for some standard technologies do not allow for a circular shape. The more popular solution for PEBP is using guard-ring that is considered in this work. To avoid the risk of device premature edge breakdown generally a guard-ring structure is implemented where the peripheral junction has a slightly doped region than the active junction because a low doped region has lower electric-field compared to a heavily doped one. Guard-rings have been used for decades to achieve several goals, including dark-current reduction in photodiodes, 1/f noise reduction in oscillators, etc. Primarily guard-ring was implemented by cleaving the junction so that only the planar junction surface remains [141]. This technique cannot be used as a standard process for large number of pixels and cannot be included in CMOS standard processes. Diffused guard-ring technique extends the region across which the electric field develops, thereby decreasing it at the edges. This technique is compatible with standard processing steps, but it occupies large space and lower the fill-factor [142], [26]. In the Mesa guard-ring [142], etching and subsequent filling with a dielectric physically planarizes and

isolates adjacent junctions. Arrays of devices using this technique are demonstrated, where fill factor and pitch are adversely impacted [142]. Field-limiting rings used in high-voltage devices to prevent PEB in curved junction regions [143]. PEB prevention is accomplished by extending the depletion region to edges where most hot spots for electric fields are expected to be located. For some previously reported CMOS APDs applied in Geiger-mode [144], [35], the guard-rings are realized with a p-well invariably with high-DCR (40kHz - 100kHz). Some of them have a buried ntype isolation layer that prevents a punch-through of the pwell guard ring to the p-substrate [35]. A similar guard-ring structure can also be created from the substrate doping by bringing rings of n-well into close proximity [145]. This device cannot be scaled much below 5μm diameter [144] because the p-well regions get so close that the active-area of the APD is almost fully depleted. The highest electric field no longer occurs at the active-area interface, and the APD performs like a planar p-well n-well diode. APDs with guard-rings formed by either n-well spacing in p-substrate or p-well implants in high-voltage wells were successful at providing low DCR [145].

Another approach is to use triple-well process steps and shallow trench isolation (STI) as a guard-ring to withstand the high electric-fields between the anode and cathode [146]. Here the edges of the drain implant are confined by the oxide trench and formation of the curved edges is prevented. As a result, a uniform field is achieved more compactly than with a diffused p-well ring. However, STI dramatically increases the density of deep-level carrier generation centers at its interface [142]. Since the active region of the SiAPD is in direct contact with the STI, the injection of free carriers into the sensitive region of the detector results in a very high DCR (~1MHz) due to the traps at the Si-SiO2 interface and degrades the performance of SiAPD. Even by considering the PEB effect and applying different PEB prevention (PEBP) techniques, only a few percent of fabricated APDs using standard CMOS technology are functional even with a proper design specifications interpreted from the theory and device simulation results before fabrication[147],[148]. In[140] we have studied the most popular applied PEBP techniques and a new practical and efficient design procedure technique is proposed in order to have a functional fabricated APD based on the simulation and fabrication experiences. The most efficient applied guard-rings are shown in Figure 3.1. In Fig. 3.1(a) the n+ layer maximizes the electric field in the middle of the diode. In Fig. 3.1(b) the lightly doped p-well implant reduces the electric field at the edge of the p+ implant.

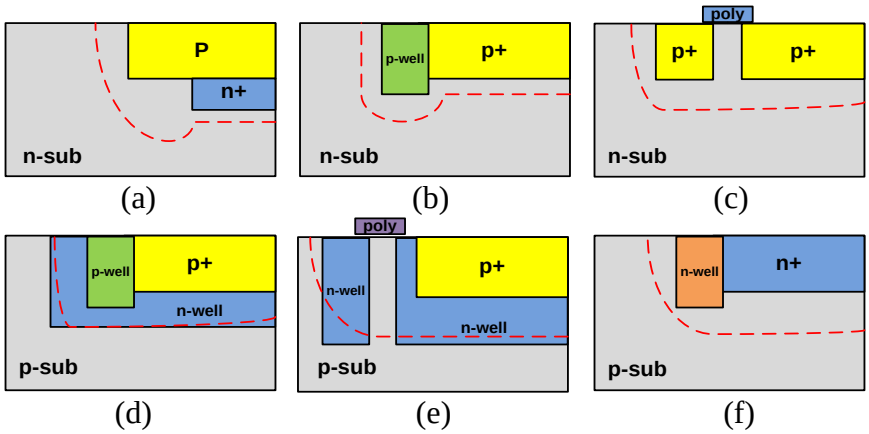


Figure 3-1: Premature edge breakdown prevention mechanisms in planar processes: (a) n+, (b) p-well, (c) n-sub, (d) p-well in p+/n-well APD, (e) p-sub, (f) n-well.

In Fig. 3.1(c) a floating p implant locally increases the breakdown voltage. With a polysilicon gate (poly) one can further extend the depletion region shown by dashed red line. In a process with trenches it is possible to decrease the electric field using the geometry of solution. When trenches are used one needs to adopt techniques to prevent that traps accumulated in the trench during fabrication can induce PEB. The trench based structure is mostly appropriate in deep-submicron CMOS technologies, where deep and medium tubs are not available without a major change in the fabrication process[149]. Due to the higher efficiencies observed based on the simulation we have focused mainly on (c)-(f) structures. The Fig. 3.1(c) and Fig. 3.1 (d) has been fabricated in 0.35 µm CMOS technology[150],[87] and the (c)-(f) in 0.18 µm CMOS technology[151].

3.4 APD Structures

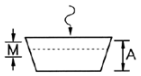
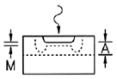
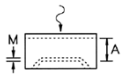
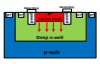
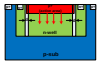
APDs can be obtained by implementing two possible approximations that produce two different structures with differentiated capabilities. On one hand, thin silicon APDs[152] are devices with a depletion layer of few micrometres and low breakdown-voltages. They also present good detection efficiency and time-resolution. As in planar APDs it is important to avoid the possibility of edge breakdown of the sensor, many different terminations have been proposed, generating a variety of planar CMOS compatible devices. On the other hand, thick APDs[153]

are devices with a depletion layer of some tens of micrometres that work at high breakdown-voltage; they have good detection efficiency but moderate time-resolution. These components are fabricated in dedicated technologies, increasing their cost[59]. Several common APD structures have been compared in Table 3.1 [154]. The Table 3.2 [59] also shows the comparison of the dedicated and planar APDs which have been explained more in detail in follow:

a. Reach-through (thick) APD: As APDs are mainly used as photo-detectors, the detection efficiency is given for wavelengths. When high-energy particles are considered, the detection efficiency is related to the number of electrons generated by ionization in the multiplication region due to the crossing particle. A method to build a thick APD using dedicated technologies consists on building the sensor on a p substrate with an n+ layer on one side and a p+ diffused layer to improve the ohmic contact on the other side [155]. This produces a reach-through structure formed by four layers in a vertical structure, generating a p+-π-p-n+ stack that can be improved through processes covered by patents [156], [157]. As its operation is based on the complete depletion of the device (30 to 100μm deep), the required voltages are high, typically over 100V. This produces sensors with low-noise and high quantum-efficiency [153], [158]. This technology allows the possibility to produce wide active-areas, up to 500 um in diameter, with variable depletion-layer thickness [159]. There are some commercial compact modules that include the bias and the quenching circuitry [160]. Although the reach-through structures have good performance, they also have some drawbacks, including the high power-dissipation (5 to 10 W) due to the high biasing-voltage and the high fabrication-cost (due to a low fabrication-yield). Furthermore, the devices are delicate and degradable, and are not integratable with circuitry.

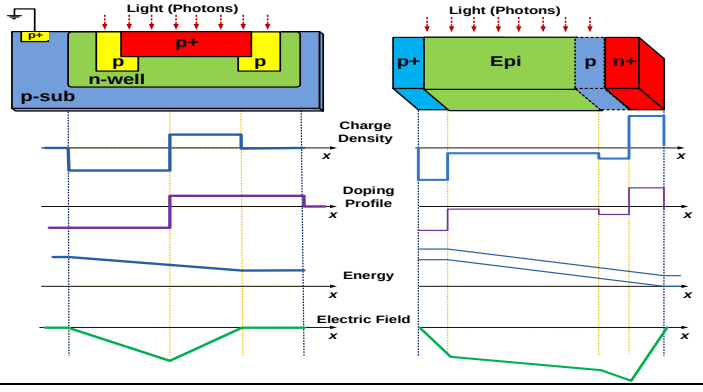
b. Planar (thin) APD: APD devices developed in planar technologies generate a thin depletion layer of few micrometers (thin APDs). These devices are generated by epitaxy over silicon wafers [161]. Over the last years, improvements of the technology to fabricate integrated circuits have allowed the development of APDs integrated in commercial CMOS technologies. Some performances are associated to these devices, such as the possibility of integrating the electronics of the detector, of developing arrays of sensors, and of using low-voltages and reducing the power-consumption of the devices. One of the main disadvantages of the utilization of standard fabrication processes is the impossibility of modifying the fabrication process without the foundry interaction, inhibiting the possibility of device optimization [31].

Table 3.1: Comparison of different APD structures.

SiAPD Type	Bevelled edge	Epitaxial	Reach-Through	PWGR[1]	PTGR[2]	NWGR[3]
Structure						
Absorption Region	large	Low	Medium to large	low	low	low
Multiplication Region	large	Low	Medium to large	50µm	50µm	50µm
Typical Size (Diameter)	<16 nm	<5 mm	<5mm	100µm	100µm	100µm
Gain	50-1000	1-100	15-300	110	130	200
Excess noise Factor	Very good (k=0.0015)	Good (k=0.03)	Good-Very good (k=0.02-0.002)	Good	Good	Very good
Operating voltage	500-2kV	80-300V	150-500 V	12V	9V	6V
Rise Time	Slow	Fast	Fast	Fast	Fast	Fast
Capacitance	Small	Large	Small	Small	Small	Small
Blue(350nm) Sensitivity	Good	Poor	Poor	Poor	Poor	Poor
Red(650nm) Sensitivity	Good	Good	Good	Good	Good	Very Good
NIR(900nm) Sensitivity	Very Good	Good	Very Good	Good	Good	Very Good

[1] p-well guard-ring APD. [2] p-sub guard-ring APD. [3] n-well guard-ring APD.

Table 3.2: Comparison of dedicated and planar APD structures.

Feature	Planar APD	Dedicated APD
Thickness	Thin	Thick
Vbr	10-50 V	100-500 V
Active Area	5-150 µm	100-500 µm
Multiplication Thickness	1-2 µm	30-100 µm
PDE	0.1%@1064nm and 45%@500nm	3%@1064nm and 95%@500nm
Jitter	<100 ps FWHM	150ps - 350ps
DCR	Technology dependent	Very low
Power Consumption	Low, No cooling required	High, Cooling Required
Array Fabrication	Compatible	Not compatible
Robustness	Good	Weak
Cost	Low	High
APD Structure		
Doping Profile		
Charge Profile		
Energy		
Electric field		

3.5 Wavelength-Specific Design

Photodetection is based on photon-absorption in semiconductor materials, which can be due to the intrinsic band-to-band, free-carrier, or band-to-impurity absorption. Intrinsic band-to-band absorption occurs when the photon-energy (Eph) is greater than the material bandgap-energy (Eg), and it is the dominant absorption mechanism in most semiconductors used for photodetection. The requirement that the photon-energy (E=*hv*) be sufficient to create an electron-hole pair (EHP) can be expressed as:

$$E_{ph} = hv = h\frac{c}{\lambda} > E_g \tag{3.1}$$

The upper cut-off wavelength (λ_g) for photo-generative absorption is therefore determined by the bandgap-energy (E_g) of the semiconductor:

$$\lambda_g(\mu m) = h\frac{c}{E_g} = \frac{1.24\mu m}{E_g(eV)} \tag{3.2}$$

Incident photons with wavelengths shorter than the upper cut-off wavelength (λ_g) become absorbed as they travel in the semiconductor. The photon-intensity decreases exponentially with the depth in the semiconductor (x) as follow:

$$N_{ph}(x) = N_{opt}e^{-\alpha x} \tag{3.3}$$

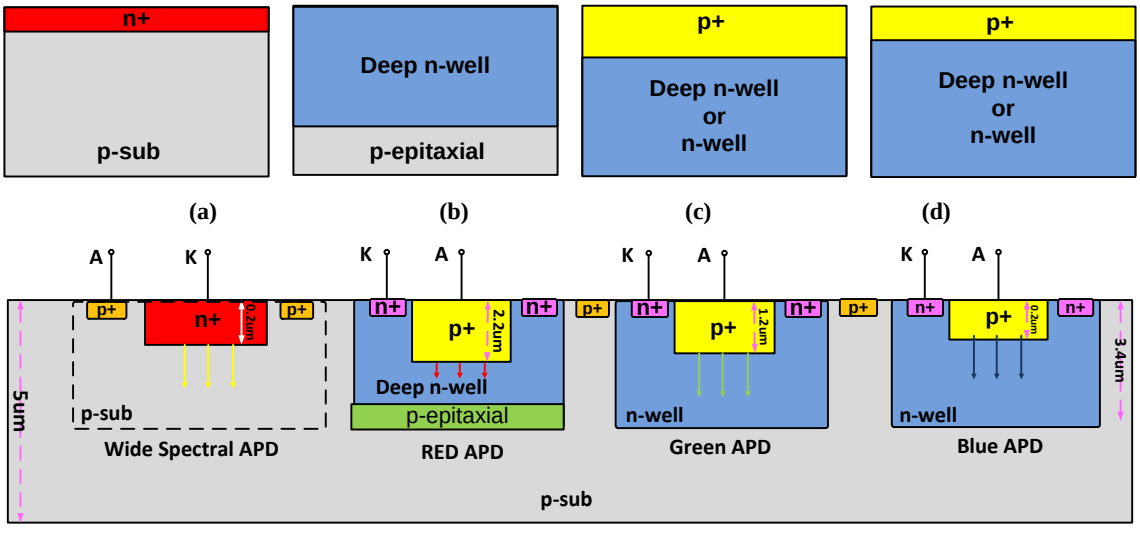


Figure 3-2: Wavelength-specific design of APD structures: (a) Wide-spectral, (b) RED-IR sensitive, (c) Green-sensitive, (d) Blue-sensitive APD structures. The doping is: $1 \times 10^{15}cm^{-3}$ for p-sub, $2 \times 10^{17}cm^{-3}$ for n-well, and $5 \times 10^{19}cm^{-3}$in n+ and p+ regions.

where α is the absorption coefficient, which depends on the photon-energy or wavelength and semiconductor material. Most of the photon absorption (~60%) occurs over a depth $\delta = 1/\alpha$ called the penetration-depth. Penetration-depth is defined at the point at which e^{-1} of the optical-power remains[162]. In order to boosts the quality of the APDs, we have to apply a wavelength-specific SiAPD design procedure. CMOS SiAPDs with wide depletion-region (>10μm) are appropriate for NIR light absorption which necessitates designing the SiAPDs with low-doped layers. The design scales for wavelength-specific design, was gained as shown in Figure 3.2 without showing the guard-rings[163]. The blue and green sensitive APD structures are p-type diffusion (P+) as a anode and n-type well (n-well) or deep-nwell as a cathode. In these structures, the junction lies between P+ and n-well/deep-nwell, and is generally quite shallow (<<1μm). Three regions contribute to the PDP. First, electrons in P+ will diffuse from P+ to the junction after absorbed light generates an electron-hole pair, possibly triggering an avalanche. Second, generated electrons or holes in the multiplication region may trigger an avalanche. Finally, generated holes by absorbed light in n-well/deep-nwell also move from nwell to the junction and may trigger an avalanche, but the impact ionization coefficient of holes is lower than that of electrons, with the PDP decreasing at longer wavelengths, because PDP is a function of the impact ionization coefficient and PDP will be lower as the impact ionization coefficient decreases. Furthermore, the impact ionization coefficient of electrons is higher than that of holes, so the peak of PDP will be biased towards shorter wavelengths of light, which generates carriers closer to the surface. The infra-red sensitive APD constructs by burying the multiplication region, and achieve high PDP for longer wavelength because generated electrons in the deep may trigger the avalanche with high impact ionization possibilities. In proposed wide spectral APD the substrate doping is too high, so the depletion region becomes small, which lead to poor PDP[163]. The penetration depth in silicon is less than 1μm for λ=400nm, less than 14 μm for λ=650nm, and higher than 14 μm for λ=850nm[164],[165].

3.6 CMOS Silicon Avalanche Photodiodes: Modeling and Simulation

In order to fabricate an APD with desired characteristics, an accurate model of the device has to be used and its characteristics should be evaluated using simulation. However the complex multi-physics characteristics of the CMOS avalanche photodiode (APD) make it difficult to develop a realistic and reliable model before fabrication. The quality metrics to design a high-performance

image sensor for low-level light detection depends on both the structure and the geometry (scale) of the photo-sensor. The APD current is generated from trap-assisted tunneling, band-to-band tunneling and avalanche impact-ionization processes respectively. In order to operate an APD in Geiger-mode, the transition between band-to-band tunneling and the avalanche must be sharp. This is usually implemented using a guard-ring. However, characterizing an APD regarding to the efficiency of the applied guar-ring based on the simulations and using available device simulators is controversial and leads to a discrepancy which is usually observed between the simulation and the experimental results. This issue can be traced to the inefficiency of the applied modeling techniques and complexity of the fabrication process. Here we have used different simulators in order to introduce the key-points and the critical design considerations towards offering a functional APD with higher efficiency after fabrication in standard CMOS technology. The main purpose of using APD circuit model was using an APD model to be applied in circuit-level simulation of the front-end circuits. Using device simulator to evaluate the characteristics of the implemented APD structures, we have investigated the electric field distribution in the APD structure under reverse bias-voltage. Using this information we have specified the places where the breakdown occurs first while the device is under reverse bias-voltage for PEB-prevention [166], [167].

Several tools are currently used for modeling and simulation of the APDs in different technologies such as COMSOL [166], TCAD[140],[168],[169],[170], MATLAB[171], Crosslight APSYS[172] and Silvaco[173],[174]. Several photo-sensors including silicon PIN photodiode and avalanche photodiodes (SiAPDs) have been addressed to develop a miniaturized near-infrared photo-sensor with high-sensitivity, low-power and low-noise characteristics using CMOS technology dedicated to biomedical imaging applications [166], [167]. These devices have been characterized and compared using different device simulators include COMSOL, TCAD, MATLAB, Crosslight-APSYS and Silvaco. The impact of simulation and reliability of the simulation results have been evaluated regarding to the measurement results [175]. The source of observed discrepancies between simulated and measured characteristics has been discussed. Then a reliable technique in order to use device simulators for APD modeling has been proposed based on our previous design, simulation and fabrication experiences [166], [167]. A new equivalent circuit model for SiAPD has been also developed in order to be applied in circuit level simulations [167].

Electric Circuit Model

Several equivalent circuits for photodiode have been proposed in the literature in order to be used in the photodetector circuits [176],[177],[178],[179]. In model depicted in Figure 3.3 (a)-(c), first the GM-APD is fully charged (armed) to a voltage above its breakdown voltage. The circuit is in this state until an internally-generated carrier triggers an avalanche. Considering the negligible leakage through the diode due to the edge-effects and the collected dark-current in the scupper areas, the voltage v_d ($v_d = v_1 - v_2$) and the current i_L can be described as:

$$v_d = \left(\frac{R_i}{R_i + R_L}\right) V_s \tag{3.4}$$

$$i_L = \frac{V_s - v_d}{R_L} \tag{3.5}$$

When a dark-carrier triggers an avalanche, the GM-APD draws exponentially, increasing current through the load-resistor until the carrier accumulation causes the current to saturate. However, the supply-voltage (Vs) divided by the load resistance (R_L) also limits this current. The current i_d is instantaneously dynamic as the GM-APD avalanches, and the GM-APD itself becomes the equivalent of a high-value current source (small resistance) in parallel with a capacitor. Here:

$$v_d = V_s - i_d R_L \tag{3.6}$$

$$V_{th} = V_s * \left(\frac{R_i}{R_i + R_L}\right) \tag{3.7}$$

$$R_{th} = \left(\frac{1}{R_i} + \frac{1}{R_L}\right)^{-1} \tag{3.8}$$

$$C_{tot} = C_d + C_1 \tag{3.9}$$

$$v_d(t) = V_{BR} * e^{\frac{-t}{C_{tot} \cdot R_{th}}} + V_{th}\left(1 - e^{\frac{-t}{C_{tot} \cdot R_{th}}}\right) \tag{3.10}$$

Once v_d decreases below the breakdown-voltage (or the current through the APD is no longer sufficient to replace the collected carriers), the free carriers in the multiplication-region of the APD will no longer have enough energy for a self-sustaining avalanche and the diode recharges due to the current flowing through R_L and the cable capacitance (C_1). The equivalent circuit for third state is the same as for the first state, with different initial conditions [71].

In order to simulate the behavior of the photodiode in our designs we have also used the equivalent circuit model shown in Figure 3.3(d). This circuit is based on the proposed circuit in [180]. The conventional PN junction diode model is used for the core of the photodiode model. R_1 represents the shunt-resistance and C is the depletion capacitance of the diode at the reverse bias condition. The C affects on the speed and the noise performance of the amplified photodetector. R2 and R3 model the series resistance at the cathode and anode side of the diode, respectively. They significantly affect on detection SNR. To account for the parasitic inductances associated with interconnection lines, L1 and L2 are added in series with R2 and R3 at the cathode and anode side, respectively. Here we have used the thermistor and a control block in order to taking in to the account the variation of the APD parameters according to the temperature, noise and bias fluctuations.

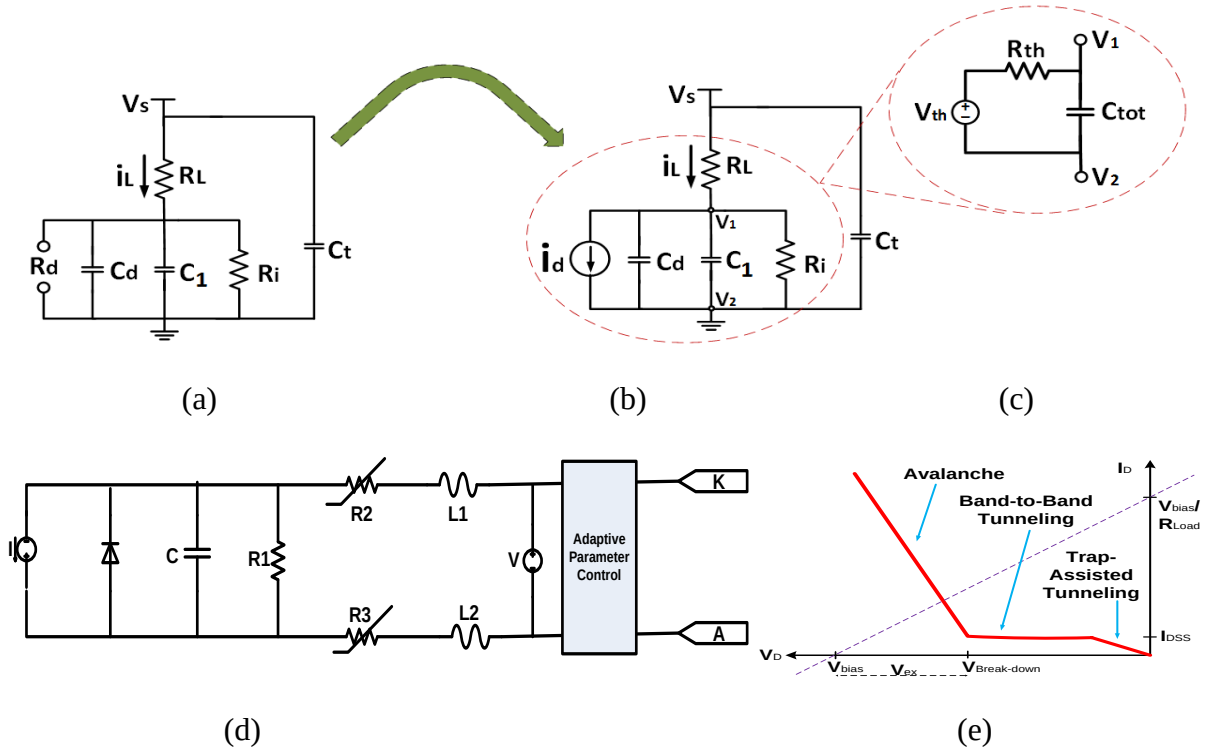
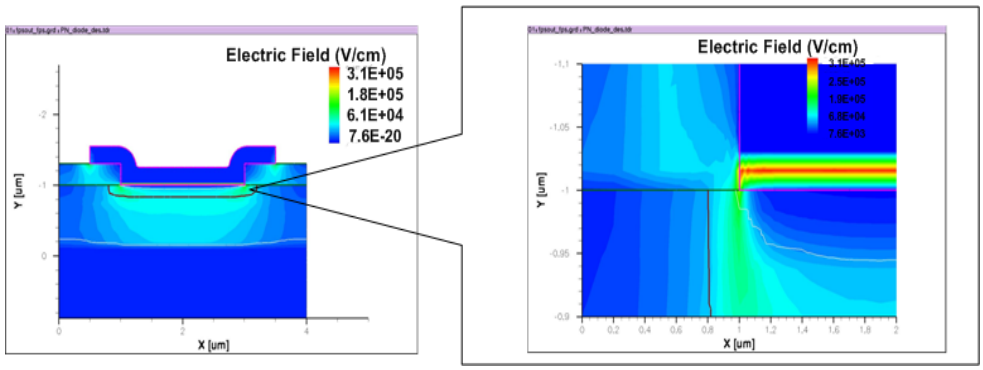


Figure 3-3: The APD equivalent circuit before avalanche (a), and after avalanche (b), and after reset (c). Here the Cd is the APD depletion-capacitance. Rd is the APD equivalent-resistance (ideally infinite) and i_d is the APD current during avalanche. The implemented equivalent circuit model of APD (d), and the I-V characteristics (e).

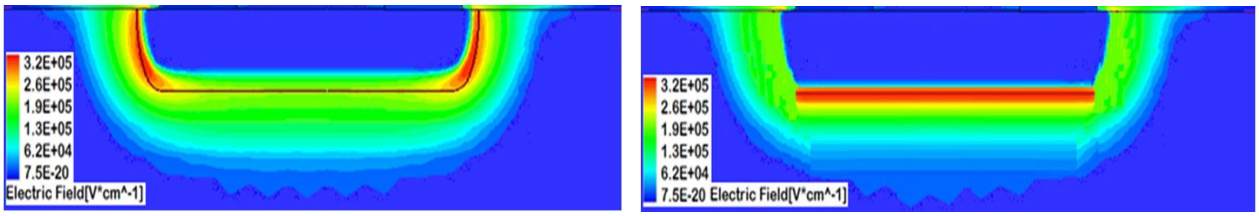
Device Simulation

We have used CADENCE schematic editor and Virtuoso layout editor for optimal design and simulation of the APD and peripheral circuitries. Optimization of the performance of SiAPD is done by device level simulation using Sentaurus TCAD software. Using a silicon avalanche photodiode (SiAPD) with an active-area of 2µm×50µm, we have studied the electric field distribution in the device under reverse bias voltage. We have created the masks for the SiAPD structure using Ligament Layout Editor and created an input command file for Ligament Flow Editor has been created. The input command file emulates the fabrication process and creates the structure and its doping data. The output from Ligament Flow Editor serves as an input for Sentaurus Process, which produces the doping-profile and the electric-field distribution of the APD. Figures 3.4(a)-(b) show the electric-field distribution of the SiAPD under reverse-bias (62V) using TCAD. It also shows that the maximum electric field (~10^5 V/cm) appeared in the active p+-deep n-well junction and the device is able to withstand the electric field without breakdown [9].



(a) (b)

Figure 3-4: The device simulation of the SiAPD under 62V reverse bias-voltage using Sentaurus TCAD (a)-(b).



(a) (b)

Figure 3-5: Device simulation of the SiAPD under reverse bias: (a) the electric distribution while no guard-ring is used. (b) Using guard-ring the maximum electric field distribution is mainly located at active region of the device under reverse bias (the first row: TCAD, the second row: COMSOL).

Figure 3.5 shows the effect of premature breakdown in the implemented SiAPDs using standard CMOS process. It should be noted that, the efficient use of modeling and device simulators in the design and characterization of the CMOS APDs plays a critical role in order to reach a functional and high-performance device after fabrication. It is recommended to use several tools by considering multiple criterias (such as I-V and electric-field distribution) in simulation. As an example, the PEB effects may not appear in the electric-field distribution but in the I-V plot.

3.7 Characterization of Silicon Avalanche Photodiodes (SiAPDs)

In order to implement the CMOS SiAPDs characterization protocol, we have developed several experimental setups. These set-ups have been used for different chips (fabricated in 0.18µm and 0.35µm technologies) experiments. The general set-ups for TIA and APD are shown in Figure 3.6. In this set-up, for the light source, different RED and NIR LEDs (600nm<λ<900nm), have been coupled to a fast pulse-generator (PDL800-B PicoQuant). The light is modulated by an electro-optic modulator and then illuminated on SiAPD through a lensed 12µm fiber-optic by positioning the fiber on top of the APD. In the optical system an LED (a Xenon lamp alternatively for wider range) is used as radiation source, the wavelength selection is performed by a Czerny-Turner monochromator (FWHM ≤ 1 nm in the 130–1100 nm spectral range) and a beam splitter directs the monochromatic radiation towards an integrating sphere that guarantees a spatial integration of the radiant flux on a 1 cm^2 reference APD and on the detector to be characterized.

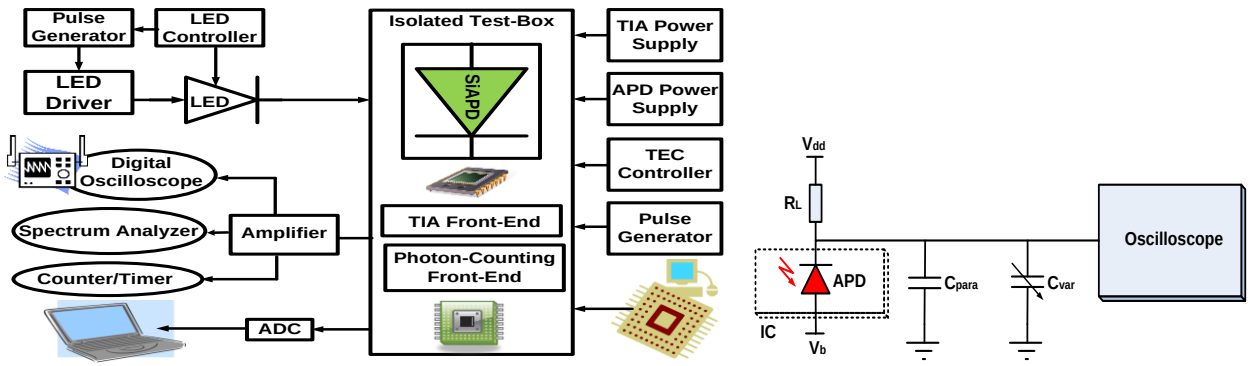


Figure 3-6: The general experimental set-up (a) and APD connection to oscilloscope configuration (b).

The calibrated photodiode allows to evaluate the number of photons per unit area, and then, after proper rescaling, the number of photons on the detectors [181]. The electronic equipment includes a counting system and an electrometer (Keithley 6154) connected to a PC (using an IEEE 488 interface) and measure the APD photo-current [182], [183]. Each APD has its own metal connection and metal pad for contact with a probe needle. In bare die measurements, the back of the wafer (substrate contact) is grounded via the probe station stage, and the probe needle provides the diode biasing by applying a positive voltage to the APD's metal pads [71]. A device wafer and a microscope-equipped wafer probe station have been also used in order to elaborate the SiAPD output signal. For continuous-light experiments, the SiAPD was directly connected to a SensL pre-amplification board including TIA (a FTA810B amplifier with gain 200 and rise time<1ns). For the pulsed-light experiments, however the SiAPD was connected to a SensL pulsed amplifier (with amplification factor of 20) followed by a Lecroy 4608 edge discriminator (with a user-defined threshold voltage to provide a triggering signal). A counting system is used for simple **dark-count** measurements and a self-correlated timing apparatus is used for afterpulse measurements. The SiAPD signal is acquired by the discriminator that generates two delayed signals, one to start and the other to stop the time-to-amplitude converter, TAC (Ortec 457). The TAC allows a tunable range between 50 ns and 5 μs.

The **photon detection efficiency** is defined as:

$$\mathrm{PDE} = \frac{\mathrm{C_R} - \mathrm{I_{dark}}}{\mathrm{N}} \approx \frac{\mathrm{I_{ph}}}{\mathrm{P_{ph}}} \cdot \frac{1.24 \times 10^{-6}}{\lambda} \qquad (3.11)$$

where I_{ph} is photocurrent, $\mathrm{P_{ph}}$ is the incident continuous-wave (CW) optical power focused in a spot in the middle of the APD photosensitive area and λ is the wavelength of the incident light, $\mathrm{C_R}$ is the count-rate at a certain incoming photon-rate $N = P_{ph}.\lambda/hc$, h is the Planck constant, and c is the speed of light. The **optical power** illuminating the detector ($P_{ph} = P_1 \times 10^{(-\alpha/10)}$) is obtained by measuring CW light-power (P_1) with an optical power meter, then attenuating the light down to single-photon level with a set of calibrated attenuators (variable attenuator and neutral density filters) providing a cumulative attenuation (a [dB]). The PDE could be further increased slightly by decapsulating the APD package, whose entrance window is not antireflection coated [184]. The PDE has been measured based on two typical techniques by measuring the photo-generated current (photo-current method) and the photon-numbers (photon-counting method). Comparison of the results from these two techniques showed a significant

PDE overestimation in the photo-current method compare to the photon-counting technique. We demonstrated unequivocally that this is essentially due to the fact that the photocurrent technique cannot discriminate the afterpulse and the cross-talk effects. On the contrary, the photon counting method allows to characterize and accurately discriminate the two noise effects providing PDE values quite close to the real ones, but needs to operate in appropriate signal conditions, in fact very fast events can be lost and the total counted events can be lower than those expected. Then we can conclude that the photon counting is a method well suited for PDE measurements because it definitely deals with true photons, reducing as much as possible the contribution of extra pulses [185].

For **cooling** and evaluation of the APD in different temperatures, it has been mounted on a thermoelectric cooler (TEC). Different 3-stage and 4-stage TECs also have been used for lower temperatures. In order to reduce the heat flow via air convection, the TEC-APD assembly was tightly surrounded with cut-to-shape Styrofoam [184]. The board (SiAPD + Amplifier) has been located in a metallic helium box sealed with grease. The **cooling** fluid has been pumped into the box through a copper pipe, allowing controlled temperature variations. The temperature of the system has been measured by a thermistor placed in contact with the external packaging of the sensor [186]. The **photocurrent** is determined by subtracting dark currents from SiAPD photodetected currents, and **avalanche gain** is defined as the ratio of photocurrents between a given bias voltage and 1V bias [56]. The precise measurement of the APD **multiplication gain (M)** is a critical requirement for APDs due to the high background and detector noise. It is calculated using following formula:

$$M = 1/(1-\int_0^L \alpha(x)dx) = 1/(1-(\frac{V}{V_{br}})^n) \qquad (3.12)$$

where L is the space charge boundary for electrons and α is the multiplication coefficient for electrons (and holes), strongly depended on the applied electric field strength, temperature, and doping profile.

Noise characterization: The main factors for the APD noise characterization include After-pulsing, Re-triggering and DCR have been considered in the experiments. The **After-pulsing** results from the release of carriers trapped in intermediate energy states (the material band gap energy). Unlike thermal carrier generation (the most prominent cause of dark-counts), the After-

pulsing is dependent on the quenching time of the device, during which the device is unable to detect a carrier. Another mechanism, called self **re-triggering**, occurs when relaxing carriers emit photons during an avalanche. These photons can be absorbed in the substrate and generate dark carriers. Self-retriggering is also dependent on the quenching time of the device. Avalanche noise is measured in terms of excess noise (F). The excess noise with pure hole injection (F_h) is equal to [19],[187]:

$$F_h(M) = M\frac{\alpha_n}{\alpha_p} + (2 - \frac{1}{M})(1 - \frac{\alpha_n}{\alpha_p}) \tag{3.13}$$

where M is the multiplication factor, and α_n and α_p are the electron and hole ionization coefficients for the material. For **DCR** measurement the discriminator was followed by a scaler timer frequency meter (IPC-3342-T: http://www.ipcel.co.uk). Given the distinct mechanisms governing the contribution of each type of carrier generated in an APD under dark conditions, a plot of the measured DCR vs the quench time associated with the active quenching setup helps to characterize the magnitude of contribution from each mechanism. For instance, if the DCR does not change significantly as a function of the quench time, then afterpulsing and self-retriggering are not significant contributors to the DCR. Conversely, a steep rise in DCR at short quench times indicates that afterpulsing is a problem in that particular device. When that rise is not consistent with afterpulsing alone, self-retriggering must be a contributor [71].

For the wavelength-specific applications also the spectral **sensitivity** of the detector should be considered. The sensitivity is calculated as the photocurrent per unit area of the photodiode for a given irradiance. The sensitivity of a PIN photodiode-based optical receiver, is calculated by [188]:

$$\mathrm{S} = \frac{\mathrm{Q}}{\mathrm{R}}\,(\mathrm{qQB} + \sigma_{\mathrm{T}}) = \frac{\lambda \times \mathrm{Q_e}}{1240} \times 100 \quad (\%) \tag{3.14}$$

where S is sensitivity (W), $\mathrm{Q_e}$ is the quantum efficiency, Q is desired Q factor (related to the desired bit error rate or BER), R is the photodiode responsivity (A/W), q is charge of an electron (C), B is receiver bandwidth (Hz) and σ_{T} is the rms thermal noise current (A) and is given by:

$$\sigma_T^2 = (\frac{4k_BT}{R_L})F_n B \tag{3.15}$$

where k_B is Boltzmann's constant (W/°K), T is temperature (°K), R_L is the receiver load resistance (Ω) and F_n is the receiver noise factor. Responsivity of the photodetector characterises

the performance in terms of the generated photocurrent I_{ph} per incident optical power P_{opt} at a given wavelength and is calculated by:

$$\Re = \frac{P_{ph}}{P_{opt}} = \frac{\eta . q}{h . \nu} = \frac{\eta \lambda (\mu m)}{1.24} \quad [\frac{A}{W}] \tag{3.16}$$

APD Capacitance: A high-level approximation for the diode capacitance is given by the bounds of $c = \frac{\varepsilon_0 \varepsilon_r A}{d}$ as calculated with the smaller and larger radius values. Applying the geometric constants of the device, the lower and higher bound for the capacitance are calculated. A better approximation of the capacitance comes from:

$$\boldsymbol{C = \frac{\varepsilon_0 \varepsilon_r (\pi {R_B}^2)}{d} + \varepsilon_0 \varepsilon_r \int_{\emptyset=0}^{2\pi} \int_{\theta=0}^{tan^{-1}\left(\frac{R_A - R_B}{d}\right)} \frac{a(\theta, \emptyset)}{h(\theta)} d\theta d\emptyset} \tag{3.17}$$

Solving numerically using the values in Eq. (3.17) yields a more precise diode capacitance value. The passive quenching experimental results cannot characterize the diode capacitance because the cable capacitance is several orders of magnitude larger than the expected diode capacitance. In the absence of inductance-capacitance-resistance (LCR) meters with the required sensitivity, the experimental values are obtained by measuring the capacitance of a larger-area diode and scaling the results [71].

3.8 Design, Implementation and Characterization of New SiAPDs: Fabrication in CMOS 0.35 µm Technology

The standard CMOS 350nm process has n-wells, one poly layer, four metal layers, and silicide block. The layers doping and depth characteristics for both TSMC and AMS 0.35µm technologies are shown in Table 3.3. However, the implemented SiAPDs have been fabricated using TSMC 0.35µm technology. This technology suffers from weak-depths and the high-doping values. Inserting narrow p-well at the peripheral junctions of APD, does not offer an efficient guard-ring in this technology because p-well in this technology is not hand-drawn and it is presented everywhere that there is no n-well. However we have solved this issue by using d-sub guard-ring explained in this chapter, in which the n-well is splitted into two n-tubs separated by a small interval *d* constituting the guard-ring. In this section the implemented APDs in standard CMOS 0.35µm technology are characterized.

Table 3.3: Estimated characteristics of the TSMC and AMS CMOS 0.35-µm technology

Layer	Depth (µm)		Doping (cm^-3)	
Technology	TSMC	AMS	TSMC	AMS
P-Sub	-	-	1.27×10^15	1.25×10^15
N-Well	1.25	1.2	1.25×10^17	1.28×10^17
P-Well	1.28	1.2	2.01×10^17	2×10^17
N+ Contact	0.24	0.2	5.01×10^19	5×10^19
P+ Contact	0.23	0.2	5.02×10^19	5×10^19

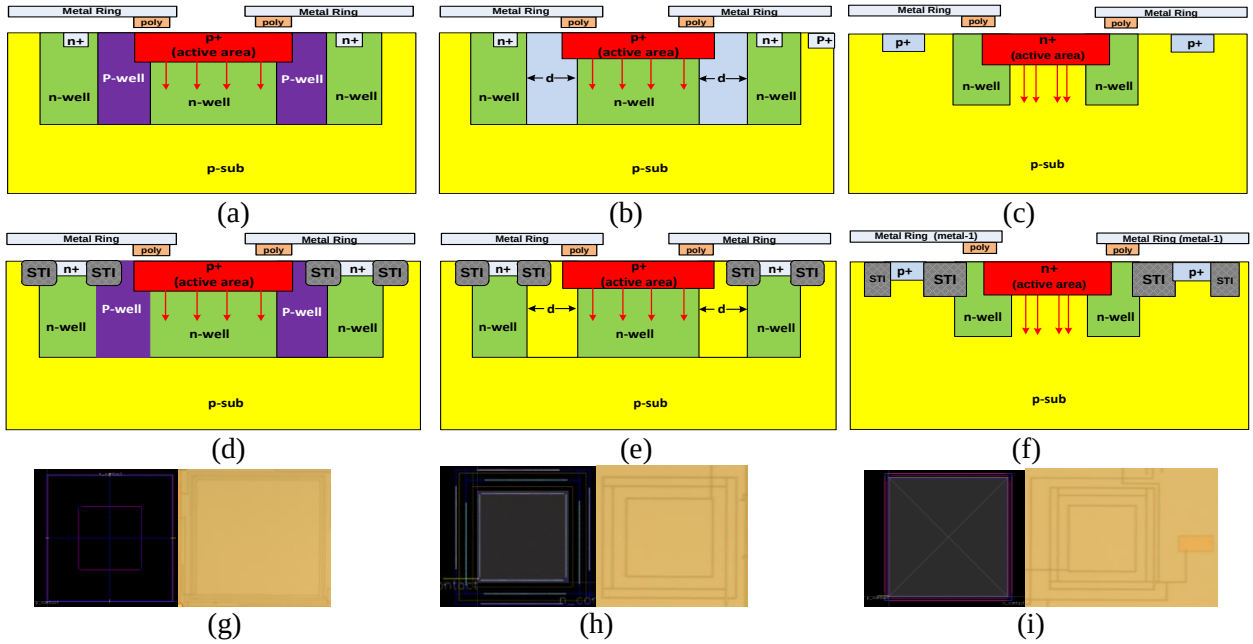


Figure 3-7: The cross-section of the fabricated APDs using standard TSMC CMOS 350nm technology. The p-well: APD1 (a), d-tub: APD2 (b), and n-well: APD3 (c) guard-rings. The same structures with STI (d)-(f). The layout-microphotograph of the APD1-3 (g)-(i).

3.8.1 p+/n-well and n+/p-sub SiAPDs

Here we have designed the **p+/n-well** SiAPDs with guard-rings in two different square and octagonal shapes, implemented using relatively low-doped layers available in standard 0.35µm CMOS technology. Schematic of the cross-section and plan-view (not to scale) of the implemented SiAPDs are depicted in Figure 3-7. The **p-well ring APD** (APD1) is a p+/n-well APD developed in square and octagonal shape (with active-area of 100µm×100µm) with a guard-ring realized by low-doped p-well around p+ active-area to preventing premature edge-breakdown. In **p-sub ring APD** (APD2), the guard-ring is realized by low-doped n-ring due to n-wells lateral diffusion. The n-well is splited into two n-tubs separated by a small interval (d≈0.9µm, which is smaller than the minimum value allowed by the design rules) constituting the

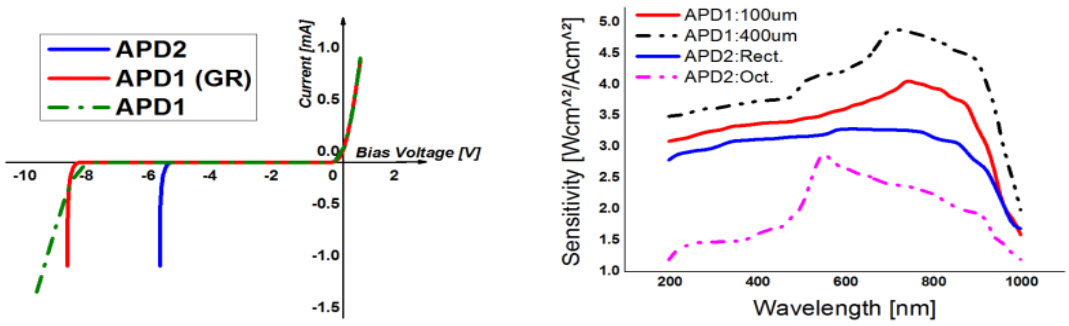
guard-ring. We have developed this APD with two different active areas of 100µm×100µm and 400µm×400µm. The third structure is an **n+/p-sub APD** (APD3), in which the guard-ring is realized using low-dopped n-well around n+. It uses the connection between the highly doped n region and the substrate as the active-region. Optimization of the performance of SiAPD is done by device-level simulation using Sentaurus TCAD, APSYS, MATLAB and COMSOL. Significant efforts have been considered in simulation stage, because the inefficiency of the applied modeling techniques accompanying with the complexity of the fabrication process can lead to a considerable dysfunctional APDs after fabrication (ex. only ~28% functional APDs by[17]). The simulation results confirmed the efficiency of the TCAD, MATLAB and COMSOL in order to imitate the I-V, breakdown and electric field distribution in CMOS APD design and characterization. Figures 3.8 (a)-(b) show the I-V and sensitivity characteristics of the SiAPDs. The sensitivity is calculated as the photocurrent per unit area of the photodiode for a given irradiance. Referring to the I-V characteristics of the proposed p-well and p-sub APDs. The general characteristics of the implemented SiAPDs are shown in Table 3.4. A significant discrepancy in photon-detection probability (PDP) and noise-factor (F) was observed in simulation using Spectra, TCAD (T) and 3DTCAD (3DT), however the extracted results from 3D-TCAD are more reliable and closer to the measurement results.

Table 3.4: Characteristics of the SiAPDs Implemented using TSMC CMOS 350nm Technology

Parameter			**Reference**	**SiAPDs**					
			No-GR	p-well GR (APD1)		d-tub GR (APD2)		n-well GR (APD3)	
				No-STI	STI	No-STI	STI	No-STI	STI
Shape	Sim./Mes.		Rect.	Rectangular	Rectangular	Rectangular	Octagonal	Rectangular	Octagonal
Area (~µm²)	Sim./Mes.		**100×100**	100 × 100	400 × 400	100 × 100	100 ×100	100 × 100	100 ×100
Linear Gain	Sim.		2	>100	100	200	100	250	120
	Mes.		-	2±1	-	3±1	-	10±8	–
PDE@700nm	Sim.		7%	85%	85%	95%	75%	98%	80%
	Mes.		-	2%±1%	-	9%±2%	-	15%±10%	-
%PDE@ 900nm	Sim.	T	1	30%	30%	40%	40%	75%	70%
		3DT	0.3	5%	45%	25%	25%	80%	70%
	Mes.		-	4%±2%	-	17%±5%	-	38%±12%	-
V_{BR}	Sim.		45	9 V	9 V	6 V	6 V	6 V	6 V
	Mes.		-	88±6	-	79±10	-	45±4	-
Impedance (Ω)	Sim.		0.1	600	600	0.5	0.5	0.5	0.5
	Mes.		0.1	810	-	0.5	-	0.5	-
Capacitance	Sim.		0.3pf	1pf	32pF	1pF	1pF	5pF	18pF
	Mes.		0.3pf	1pf	-	1pF	-	5pF	-
F@M=20	Sim.	T	-	70@800nm	95@800nm	50@800nm	74@800nm	40@800nm	73@800nm
		3DT	-	74@800nm	85@800nm	60@800nm	85@800nm	45@800nm	70@800nm

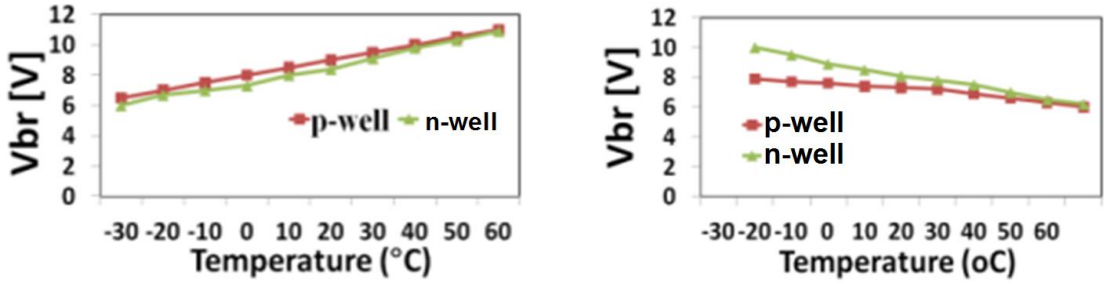
Sim.: Simulation Result; Mes.: Measurement Result; T: TCAD; 3DT: 3D-TCAD; STI: Shallow-Trench Isolation guard-ring

Since the doping concentrations for layers are fixed for the standard CMOS process, the precise implementation of the predefined optimal doping-profiles (extracted from analytical calculation and simulation) is not possible in standard CMOS technology. So the measurement results of the fabricated APDs as expected did not exactly matched with the simulations and in some fabricated APDs also there was a significant discrepancy between the simulated and measured parameters, especially regarding to the photon-detection efficiency (PDE) and dark-current. In addition to the the inadequacy of the applied device simulation tool and inflexibility of the standard CMOS technology regarding to the precise simulation and implementation of the considered characteristics, the other source of this mismatched could be due to effects of the used bonding pad parasitic capacitance and the passivation layer imposed by fabrication on the performance of the designed APDs. It also might be due to the limited accuracy of the test setup used to get these values. The **output impedance** of the SiAPD should be considered for impedance-matching with the integrated front-end amplifier. The output impedance of APD2 under reverse bias is around 0.5Ω and for the APD1 is around 600Ω. The **capacitance** of the photodetector increases with its area (1pF for a 100µm² SiAPD and 32pF for 400µm² SiAPD). For APD1 and APD2 the breakdown happens at approximately 9V and 6V respectively. The avalanche-noise is measured in terms of excess-noise (indicated by F). For the wavelength-specific applications the spectral-sensitivity of the detector also should be considered.



(a) (b)

Figure 3-8: The simulated I-V characteristics (a), and Sensitivity (b) of the SiAPDs.



(a) (b)

Figure 3-9: The breakdown-voltage variation in different temperatures: The breakdown due to avalanche (a) and tunneling (b).

The effect of doping and scale variations has also been studied. It shows that the thicker and deeper guard rings show better performance offering higher PDE and lower noise with less active area. The proposed structures have also been implemented using shallow-trench isolation (STI) guard-ring as shown in Figure 3-7 (d)-(f). The simulation results regarding to characterization of this APD demonstrate a significant noise have been added using this technique. This is due to the traps at the Si-SiO2 interface in STI structure which degrades the performance of APD. The breakdown voltage of APDs at temperature T is equal to:

$$V_{br} = V_{bias}[1+\beta(T - T_0)] \tag{3.18}$$

where β is temperature coefficient of the breakdown voltage. In order to find out if the source of the breakdown is avalanche or it is due to the tunnelling we have measured the breakdown variation in different temperatures. The value of temperature coefficient of the breakdown voltage is positive for diodes with avalanche breakdown and negative for diodes with tunnelling breakdown (Figs. 3.9 (a)-(b)).

3.9 Design, Implementation and Characterization of New SiAPDs: Fabrication in CMOS 0.18 µm Technology

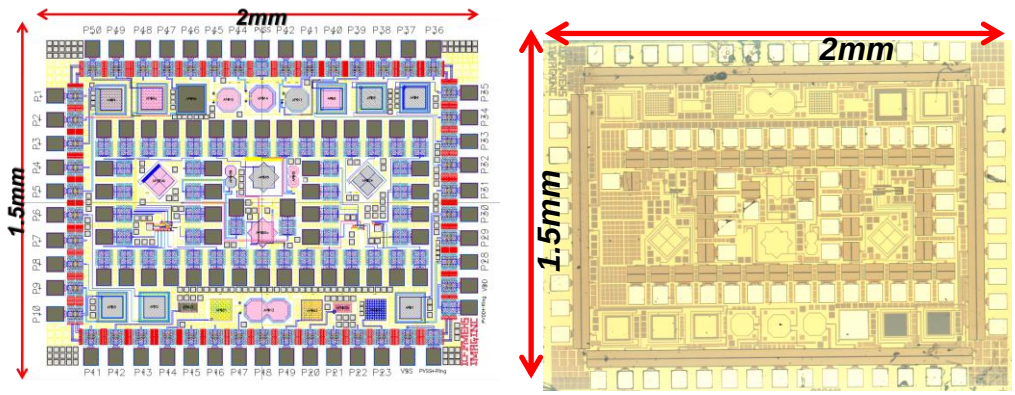
3.9.1 Design Overview

The TSMC CMOS 0.18µm process has n-wells, thin and thick oxide transistors, one polysilicon layer, six metal layers, and silicide block. The 1P6M CMOS 0.18µm offers both N-well and P-well, in which the P-well can be implemented inside a deep N-well surrounded by an N-well

layer. This technology allows circuits that can be operated on two power supplies, 1.8V and 3.3V for thin and thick oxide devices respectively. Usually 1.8V is used for the core circuit, however 3.3V is used to power-up the I/O pads, however, it is possible to power the core circuit with 3.3V at the cost of using larger transistors. The estimated characteristics of the TSMC and AMS CMOS 0.18µm technology are shown in Table 3.5. Here we have designed and implemented new SiAPDs using standard CMOS 0.18µm, fabricated by TSMC via CMC Microsystems. It includes 24 different SiAPDs in 7 new structures and shapes. A resist protection oxide (RPO) layer is used on the photosensitive areas for salicide protection. It has a total die size of 1.5mm × 2 mm and 98 pins providing access to bias, measure and monitoring of different design nodes. The layout and microphotograph of the implemented IC are shown in Figure 3-10. It has been packed in two different DIP and PGA configurations. The general electrical characteristics of the devices have been evaluated in Polystim neurotechnologies laboratory in Montreal, Canada and the optical characteristics have been evaluated at Bio-Optics Laboratory at MIT and the Harvard-MIT Division of Health Sciences and Technology (HST) in Boston, USA. In follow we have explained the main characteristics of the implemented SiAPDs.

TABLE 3.5: Estimated characteristics of the TSMC and AMS CMOS 0.18-µm technology

Layer	**Depth (µm)**		**Doping (cm^-3)**	
Technology	TSMC	AMS	TSMC	AMS
P-Sub	-	-	1.21×10^15	1.14×10^15
N-Well	1.39	1.7	1.09×10^17	1.19×10^17
P-Well	1.44	1.7	1.65×10^17	1.78×10^17
N+ Contact	0.36	0.4	4.98×10^19	4.30×10^19
P+ Contact	0.30	0.4	5.0×10^19	4.38×10^19



(a) (b)

Figure 3-10: The layout (a) and the microphotograph (b) of the integrated circuit developed using TSMC 0.18µm CMOS technology.

3.9.2 Rectangular p+/n-well SiAPDs without Guard-Ring

There is a larger depletion region and the deeper junction in **n-well/p-sub** and **p+/n-well/p-sub** and the pinned detector surface in p+/n-well/p-sub APDs [145], [189], [190]. The cross-section, layout and the microphotograph of the implemented p+/n-well SiAPDs are shown in Figure 3.11. These three APDs (named APD1-3 and APD6) are in rectangular-shapes with an Active-area = 100µm×100µm. This structure is similar to the typical pn-junction topology introduced in [145], [191], [192]. Here no guard-ring is used and the depletion-region is placed around p+ region within n-well area. Using these APDs, we could study the impact of PEB on the device behavior. Furthermore, the effect of using poly under contacts has been verified by using a poly layer under all contact (APD2), and only under the anode contact (APD3). The poly-silicon (using a poly-ring around the periphery defining a thin oxide region) applied to prevent STI creation near the active region and to move STI out of the active region. It also reduces the after-pulsing significantly. The hypothesis was using poly-gate in the proposed guard-rings where no STI is implemented, can reduce the DCR due to the partial transparency and low transmittance of poly-silicon at short wavelengths. The poly-gate has a suitable structure to accumulate and transfer carriers. Biasing the poly-silicon layers on top of the SiAPD produces a depletion region which acts as an accumulation region for photo-generated carriers and it can also increase the lifetime of the SiAPD. The current-voltage relationships are shown in Figure 3.12(a).

The p+/n-well APD is also implemented in octagonal-shape (APD7) with an active-area = 100µm×100µm. An octagonal-shape p+/p-sub APD (active-area = 100µm×100µm.) is also developed using n-well guard-rings (APD8). The cross-section, layout and microphotograph of these APDs are shown in Figure 3.11. The simulation and experimental results of these APDs are summarized in Table 3.6.

In order to measure the multiplication-gain, the APD is lighted with a stable, continuous, light source (blue LED) and the current flowing trough it (I_{on}) is measures as a function of the bias-voltage as shown in Figure 3.12 (b). The same measure is repeated while turning off the LED (I_{off}). The Gain then is calculated as:

$$G(V) = \frac{I_{on}(V) - I_{off}(V)}{I_{on}(G=1) - I_{off}(G=1)} \tag{3.19}$$

The multiplication-gain can also be measured as absolute ratio of the voltage amplitudes in the APD output signals before and after the breakdown. The general characteristics of these implemented SiAPDs, are listed in Table 3.6. As it was expected without using guard-ring, a significant percent (~80%) of the fabricated APDs didn't offered multiplication gain and weren't functional. However, in 20% cases we observed small multiplications in current and we were able to measure the Vbr values as shown in the Table 3.6. Referring to the results, using poly-gate in the implemented structure, where no STI is implemented, a significantly lower-DCR (~50%) accompanied with a trivial reduction in sensitivity were observed.

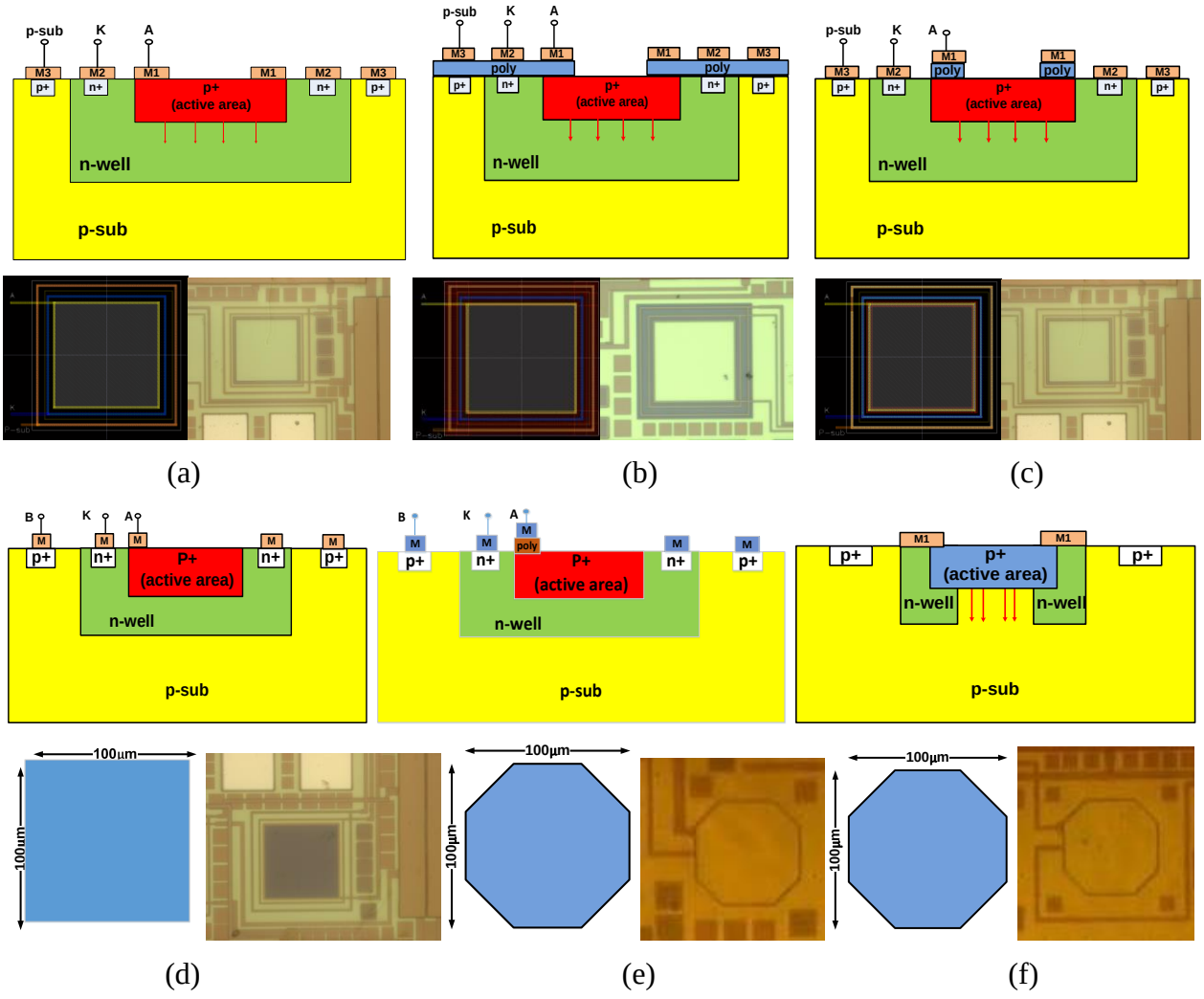
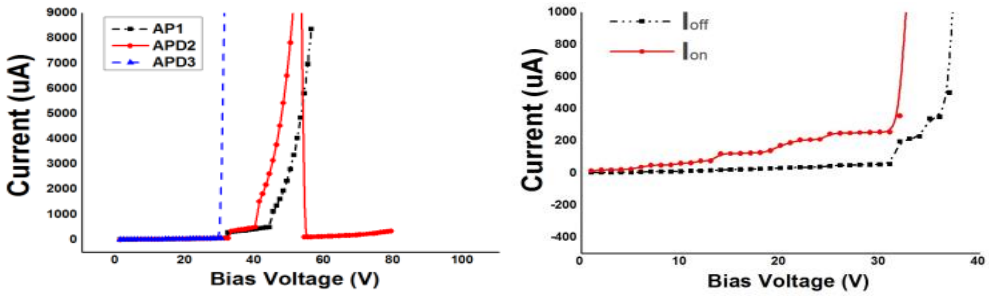


Figure 3-11: The cross-section (first row), the layout (second row), and the microphotograph (third row) of the fabricated APD1 (a), APD2 (b), and APD3 (c), APD6 (d), APD7 (e), and APD8 (f) using TSMC 180nm CMOS technology.



(a) **(b)**

Figure 3-12: The I-V characteristics of APD1-3 (a), and the multiplication-gain measurement technique (b).

Table 3.6: Specifications of the rectangular p+/n-well SiAPDs fabricated using TSMC CMOS 180nm technology (Area=100×100 μm^2)

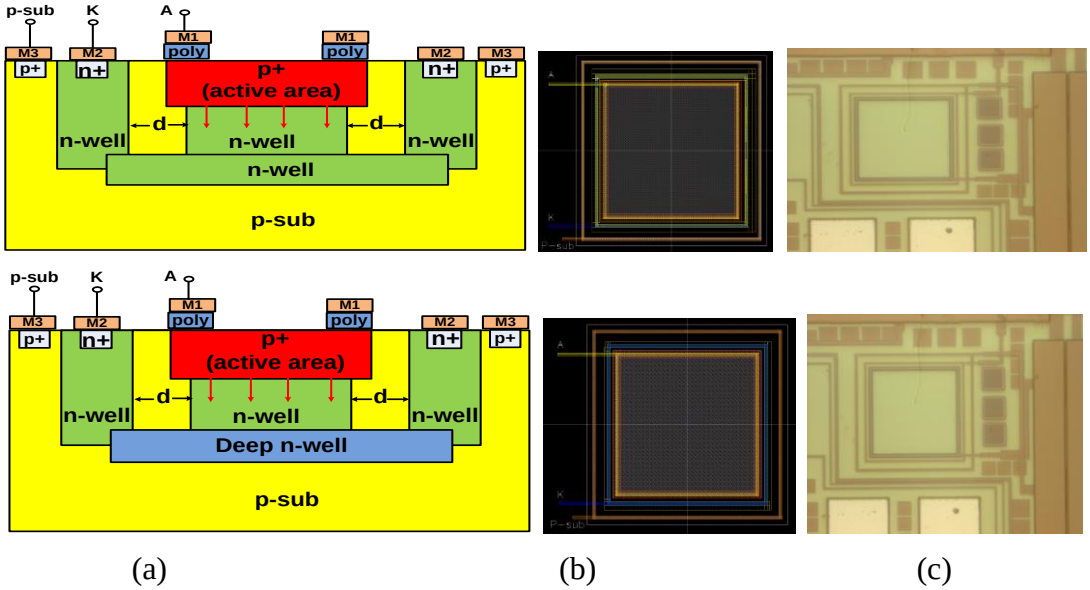
APD	Data source	Gain (M)	PDE@ 700nm	Impedance (Ω)	Capacitance	F @ M=2*	Breakdown Voltage (V)	DCR @ T=25°C	Functional SiAPDs %
APD1	Simulation	10	8%/11%	600	1 pF	97/99	32	**100kHz@Vex=1.7V**	---
	Measurement	**3±0.3**	7±1%	630±3.7	1±0.00 pF	-	32±3.5	**100±1kHz@Vex=1.7V**	10
APD1+STI**	Simulation	12	**15%/21%**	600	1 pF	**170/179**	32	**240kHz@Vex=1.7V**	---
APD2	Simulation	10	8%/11%	600	1 pF	97/99	32	**100kHz@Vex=1.7V**	---
	Measurement	**3±0.3**	7±1%	630±3.7	1±0.00 pF	-	32±3.5	**100±1kHz@Vex=1.7V**	9
APD2+STI	Simulation	12	**15%/21%**	600	1 pF	**170/179**	32	**238kHz@Vex=1.7V**	---
APD3	Simulation	10	8%/11%	609	1 pF	97/99	32	**80kHz@Vex=1.7V**	---
	Measurement	**4±0.1**	7±1%	610±3.7	1±0.00 pF	-	30±3.5	**80±1kHz@Vex=1.7V**	11
APD3+STI	Simulation	12	**15%/21%**	611	1 pF	**176/182**	32	**200kHz@Vex=1.7V**	---
APD6	Simulation	10	5%/2%	600	1 pF	70/79	49	100kHz@Vex=1.7V	---
	Measurement	2±1	2±1%	630±3.7	1±0.00 pF	83±1	89±3.5	**100±1kHz@Vex=1.7V**	7
APD6+STI	Simulation	14	25%/21%	600	1 pF	70/79	50	140kHz@Vex=1.7V	---
APD7	Simulation	17	20%/18%	0.5	1 pF	50/59	49	4kHz@Vex=1V	---
	Measurement	2±1	3±2%	0.8±0.18	1.3±0.1 pF	61±0.1	89±3.1	4±1kHz@Vex=1V	6
APD7+STI	Simulation	19	20%/18%	0.5	1 pF	50/59	49	7kHz@Vex=1V	---
APD8	Simulation	32	35%/30%	0.5	0.5 pF	36/40	41	40Hz@Vex=1V	---
	Measurement	2±1	7±2%	0.5±0.02	0.6±0.03 pF	41±0.01	56±2	40±4Hz@Vex=1V	6
APD8+STI	Simulation	32	35%/30%	0.5	0.5 pF	36/40	46	1kHz@Vex=1V	---

*In 790nm. ** Shallow-Trench Isolation guard-ring.

3.9.3 Rectangular p+/n-well SiAPDs with p-sub Guard-Ring

The cross-section of the implemented p+/n-well SiAPDs are shown in Figure 3.13. Here no explicit guard-ring is added. In other words, spacing between the active region and n-wells is achieved by substrate intrinsic doping. This structure is based on connecting n-wells surrounding an island of substrate as guard-ring. This structure performs as a p-well/n-well diode with a depletion region confined within the area between p+ and n-wells (also deep n-well in APD5). In a single-tub CMOS process, the guard-ring cannot be realized by inserting a narrow p-well at the peripheral junction since p-well layer is not hand-drawn and is present everywhere that there is no n-well. The solution is to split the n-well into two n-tubs separated by a small interval d

constituting the guard-ring. A minimum n-wells separation results in a guard-ring region doped as intrinsic substrate [42], [46], [191], [193]. The rectangular-shape p+/n-well SiAPDs with an active-area = 100µm×100µm and a d-tub guard-ring are implemented using standard CMOS process (Figure 3.13). In these APDs, the n-well is cleaved into two n-tubs separated by a small interval (d≈0.9µm) constituting the guard-ring (so they called p-well or d-tub based guard-ring SiAPD). Here in order to confine the avalanche area under the active are in APD4, a deep n-well layer is also implemented under active-area between n-well and p-sub as shown in APD5 structure. In APD5 the deep n-well (DNW) is used to connect two n-wells and isolate the guard-ring between the n-wells. A complete DNW increases the tunneling and PEB, so eliminating the DNW below the multiplication-region cause the DNW to act as a guard-ring by reversing the surrounding region onto a lightly n-doped region [42]. Here the maximum electric-field is occurring in the active-area which is required for a highly-sensitive APD operation [194]. In order to verify the impact of using deep n-well, both APDs have been fabricated and evaluated. The only different between these APDs is replacing the n-well layer in APD4 with deep n-well layer under the active area and between n-well and p-sub in APD5 as shown in Figure 3.13. The measurement and simulation results on characterization of these SiAPDs are summarized in Table 3.7. The results demonstrate that the APD5 offer a lower noise-factor, higher-gain and higher functionality compared to APD4.



(a) (b) (c)

Figure 3-13: The cross-section (a), the layout (b), and the microphotograph (c) of the fabricated APD4 (first row) and the APD5 (second row), fabricated in TSMC CMOS 180nm technology.

Table 3.7: Main specifications of the rectangular p+/n-well SiAPDs with p-sub Guard-Ring, fabricated using TSMC CMOS 180nm technology (Area=100×100 μm^2)

APD	Data source	Gain (M)	PDE @700nm	Impedance (Ω)	Capacitance	F @ M=20*	Breakdown Voltage (V)	DCR	Functional SiAPDs%
APD4	Simulation	100	**25%/21%**	600	1 pF	70/79	12	100kHz@Vex=1.7V	---
	Measurement	**31±8**	20±1%	630±3.7	1±0.00 pF	83±1	12±6	**100±1kHz@Vex=1.7V**	46
APD4+STI	Simulation	105	**25%/21%**	600	1 pF	70/79	12	140kHz@Vex=1.7V	---
APD5	Simulation	102	**20%/18%**	0.5	1 pF	50/59	11	98kHz@Vex=1V	---
	Measurement	**35±10**	15±3%	0.8±0.18	1.3±0.1 pF	**61±0.1**	12±3	**114±1kHz@Vex=1V**	67
APD5+STI	Simulation	107	**21%/18%**	0.5	1 pF	50/59	10	171kHz@Vex=1V	---

*In 790nm. ** n+/p-sub APD structure with Shallow-Trench Isolation guard-ring.

3.9.4 Rectangular/Octagonal n+/n-well and n+/p-sub SiAPDs

This structure includes 2 junctions, the n+/p-substrate and the n-well/p-substrate junctions. The main difference between the n+/p-substrate and the n-well/p-substrate junctions is the width of the depletion region. Due to the much lower doping-levels of the n-well compared to the n+ region, the width of the n-well/p-substrate depletion-region is larger, resulting in a more efficient photodetection. In terms of design rules, this structure is very compact (the fabrication design rules require larger minimum sizes and separation for n-wells) and simple compared to the other structures. It is formed by creating a highly-doped n region in the p-substrate. Due to the high doping-concentration of the n+ implant (compared to an n-well diffusion), from $W = \sqrt{\frac{2\epsilon(V_b - V)}{q}(\frac{1}{N_a} + \frac{1}{N_d})}$, the depletion-region width (W) is small. This leads to a reduction in the collection-efficiency and a large junction capacitance ($C_j = \epsilon\frac{A}{W}$) which offers a low charge-to-voltage conversion. Since the n region is created by ion implantation, the junction is relatively close to the surface. This causes a further reduction in the collection-efficiency (especially for longer wavelengths).

The APD6-7 use the lightly doped n-well diffusion to create a pn junction in the p substrate. The lower doping concentration of the n-well (compared to an n+ implant) increases the depletion width W and so reduces the junction capacitance. The larger depletion-region leads to a better collection-efficiency and the smaller capacitance improves the charge-to-voltage conversion. Since the n-well diffusion is deeper than an n+ implant, the junction is deeper and more efficient at capturing long-wavelength photons compared to a n+/p-sub junction. The increased depth also creates significant depletion-regions along the sidewalls of the junction, further improving the collection-efficiency. However, this increased junction-area, caused by higher sidewalls due to

the deeper junction, will also increase the junction capacitance C_j, offsetting some of the improvement in the charge-to-voltage conversion resulting from the smaller W. Design rules require larger minimum spacing and minimum widths for n-wells compared to n+ regions. Thus, given a constant size, a pixel with an n-well photodiode will have a lower fill factor than one with an n+/p-sub photodiode [42], [189], [191], [195]. In APD12 which is an n+/p-sub SiAPD, the guard-ring is simply developed by n-well at the peripheral junctions (n-well SiAPD). It uses the connection between the highly-doped n region and the substrate as the active-region. The n+/p-well structure, allows smaller diode implementation since the case of merging depletion layers by approaching the p-well guard-rings in p+/n-well structure, no longer happens [191]. The n+/p-well diode structure also has a lower device parasitic capacitance comparing to the p+/n-well APD (the n-well has a larger capacitance to the substrate, while the n+ layer has a much smaller capacitance to p-well) and the avalanche-area is confined only under the n+ region. The n+/n-well SiAPDs are implemented in rectangular (APD9) and octagonal (APD10) shapes as shown in Figure 3.15. The active-are is 100µm×100µm. Here the APD layout is covered with metal-2 layer as a shield to block photons from reaching the substrate. The rectangular APD11 is with the same topology with APD9, however its active-area is covered by pad. The proposed n+/p-sub rectangular SiAPD (APD12) is shown in Figure 3.15. It is implemented using n-wel guard-ring and its Active-area = 100µm×100µm. A novel double-Octagonal structure is proposed and implemented as shown in Figure 3.16. The APD13 is a n+/p-sub double-Octagonal SiAPD with Active-area= 100µm×200µm. Here, the APDs are separated in the middle with a small distance (d=10µm). The APD14 is also a novel double-Octagonal n+/p-sub structure with Active-area= 50µm×100µm (d=1µm). These ADPs have been characterized regarding to the I-V, PDP, noise and Vbr and the results are depicted in Figure 3.17 and Table 3.9.

The n-well SiAPD offers a relatively low dark current (<~100nA) generated by tunneling and Shockley-Read-Hall (SRH) processes. The SRH is strongly proportional to temperature variation comparing to the respectively week and inverse dependency of tunneling and after-pulsing. Tunneling and SRH dark counts are isolated and independently measured by varying the temperature, so that below a certain temperature, tunneling DCR dominates and above that temperature the SRH dominates, which it may impose a slight increase in power consumption at high illuminations. The STI formation is known to introduce defects and crystal lattice stresses which cause high DCR. So it is normally important to move the trench away from the main

SiAPD p-n junction. The poly-silicon (using a poly ring around the periphery defining a thin oxide region) applied to prevent STI creation near the active region and to move STI out of the active region. It also reduces the after-pulsing significantly [2], [10]. Using poly-gate in the proposed guard-rings where no STI is implemented, we still observed a significantly lower DCR (~50%) accompanying with a trivial reduction in sensitivity. This may be due to the partial transparency and low transmittance of poly-silicon at short wavelengths. The poly-gate has a suitable structure to accumulate and transfer carriers. Biasing the poly-silicon layers on top of the SiAPD produces a depletion region which acts as an accumulation region for photo-generated carriers and it can also increase the lifetime of the SiAPD. A high tunneling is expected in high Vex values due to the applied relatively highly doped substrate in this SiAPD. We have examined the effect of doping and scale variations in order to optimize the SiAPD performance. While the breakdown voltage is reduced in higher CMOS technologies due to the higher doping levels, the noise also becomes generally lower. One of the reasons is that the ionization coefficient ratio (k) is closer to unity, so the noise due to electron-hole initiated avalanche is lower. However with the downscaling of the technology, the dark-current increases. This is due to the increase in the doping concentration which increases the emission rate of carriers by the electric fields from the traps. Furthermore the quantum efficiency is also reduced due to the reduction of the absorption-region depth and an increase of the dark current due to the contribution of tunneling. However the thickness of the n-wells is constrained by design rules, our investigations based on the simulated and implemented structures, show that the thicker and deeper guard rings show better performance. The high doping values and shallow depths imposed by the applied technology constraint the technical design to reach desired high detection efficiency.

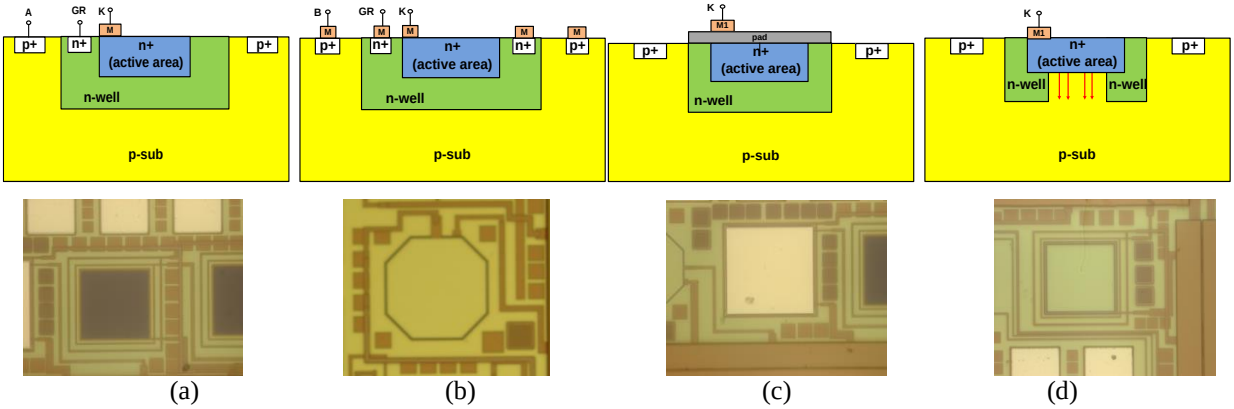
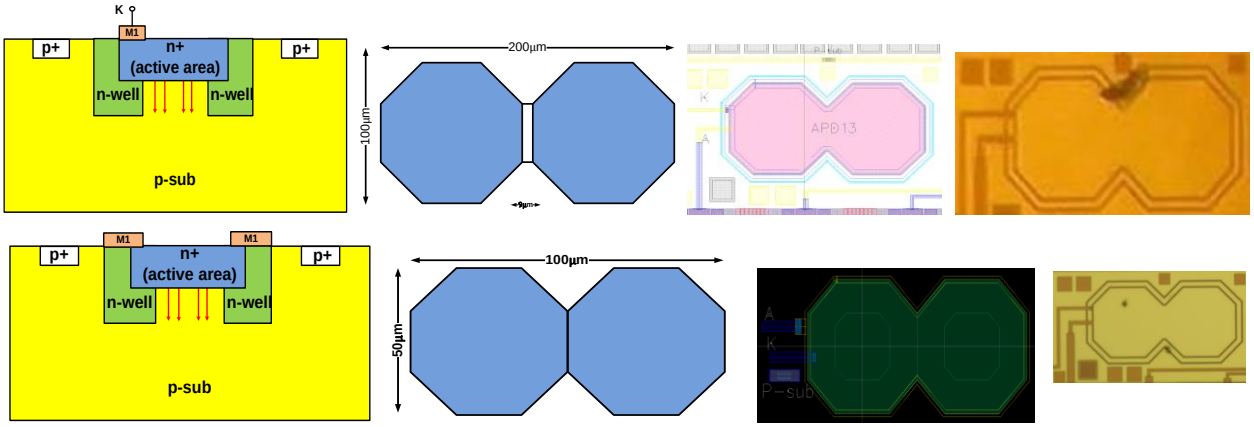
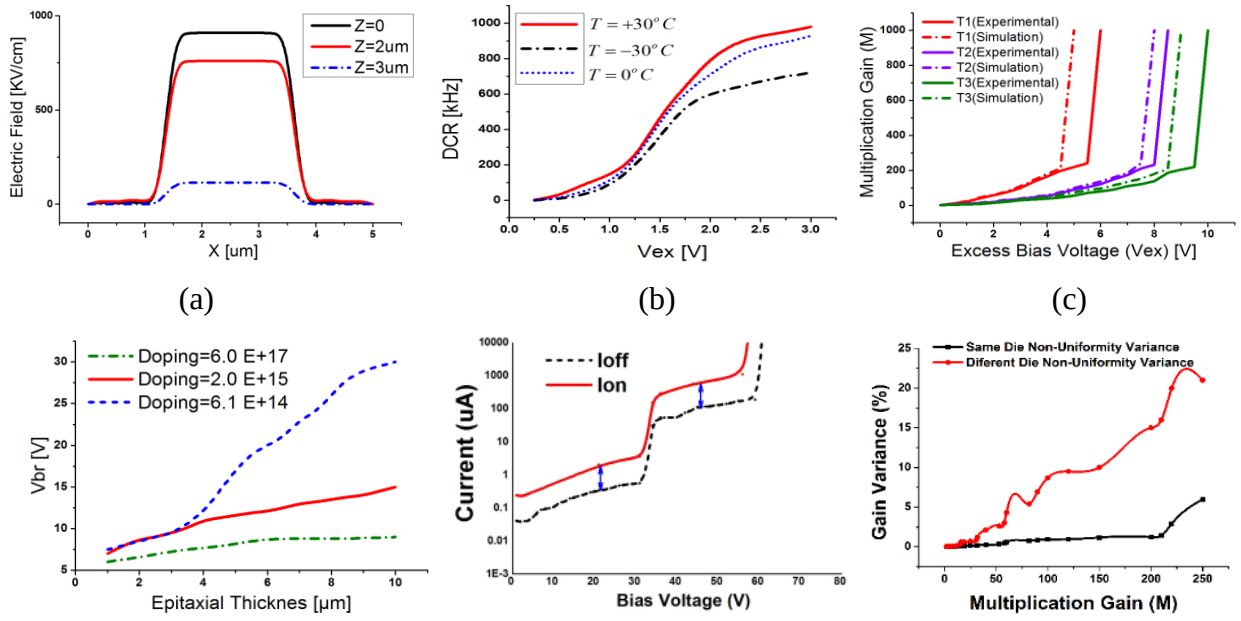


Figure 3-14: The cross-section (first row), and the microphotograph (second row) of the fabricated APD9 (a), APD10 (b), APD11 (c) and APD12 (d), fabricated in TSMC CMOS 180nm.



(a) (b) (c) (d)

Figure 3-15: The cross-section (a), the top view (b), the layout (c), and the microphotograph (d) of the fabricated APD13 (first row) and APD14 (second row), fabricated using TSMC CMOS 180nm technology.



(a) (b) (c)

(d) (e) (f)

Figure 3-16: The n-well guard-ring based SiAPD characterization: The electric field distribution (a), DCR-Vex variation (b). The M-V plot in different temperatures where $T_1 = -25^0C, T_2 = -25^0C, T_3 = -25^0C$ (c), and the TCAD simulated Vbr dependence on the epitaxial layer thickness in different epitaxial p-type doping (d). The multiplication gain measurement (e), the Gain uniformity between APDs fabricated on the same die and on different dies in the same production batch (f).

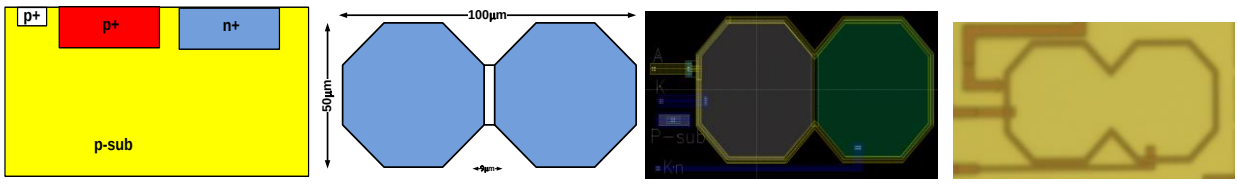
Table 3.8: Main specifications of the Octagonal n+/n-well and n+/p-sub SiAPDs, fabricated using TSMC CMOS 180nm technology (Area=100×100µm^2)

APD	Data source	Gain (M)	PDE @ 700nm	Impedance (Ω)	Capacitance	F @ M=3*	Breakdown Voltage (V)	DCR	Functional SiAPDs%
APD9	Simulation	20	**21%/21%**	700	4.3 pF	180/79	62	**100kHz@Vex=1.7V**	---
	Measurement	3±2	4±1%	630±3.7	1±0.00 pF	83±1	92±3.5	**100±1kHz@Vex=1.7V**	76
APD9+STI	Simulation	18	**25%/21%**	600	1 pF	70/79	72	**140kHz@Vex=1.7V**	---
APD10	Simulation	15	**17%/11%**	0.5	1 pF	50/59	79	4kHz@Vex=1V	---
	Measurement	**6±4**	9±2%	0.8±0.18	1.3±0.1 pF	61±0.1	89±3.1	4±1kHz@Vex=1V	67
APD10+STI	Simulation	15	**20%/18%**	0.5	1 pF	50/59	79	7kHz@Vex=1V	---
APD11	Simulation	17	**85%/70%**	0.5	0.5 pF	36/40	86	40Hz@Vex=1V	---
	Measurement	4±2	14±2%	0.5±0.02	0.6±0.03 pF	**41±0.01**	106±2	40±4Hz@Vex=1V	91
APD11+STI	Simulation	17	**15%/17%**	0.5	0.5 pF	36/40	86	1kHz@Vex=1V	---
APD12	Simulation	39	**34%/37%**	600	1 pF	70/79	12	100kHz@Vex=1.7V	---
	Measurement	20±8	24±1%	630±3.7	1±0.00 pF	83±1	42±3.5	**100±1kHz@Vex=1.7V**	76
APD12+STI	Simulation	35	31%/34%	600	1 pF	70/79	12	**140kHz@Vex=1.7V**	---
APD13	Simulation	110	45%/41%	600	1 pF	6/7	10	**100kHz@Vex=1.7V**	---
	Measurement	45±5	34±1%	630±3.7	1±0.00 pF	83±1	19±3.5	**100±1kHz@Vex=1.7V**	73
APD13+STI	Simulation	104	**45%/41%**	600	1 pF	17/21	12	**140kHz@Vex=1.7V**	---
APD14	Simulation	122	**75%/71%**	600	1 pF	7/7	10	**100kHz@Vex=1.7V**	---
	Measurement	**50±4**	64±1%	630±3.7	1±0.00 pF	8±1	22±3.5	**100±1kHz@Vex=1.7V**	87
APD14+STI	Simulation	102	**74%/71%**	600	1 pF	17/19	12	**140kHz@Vex=1.7V**	---

*In 790nm. ** n+/p-sub APD structure with Shallow-Trench Isolation guard-ring.

3.9.5 Hybrid Octagonal n+p+/p-sub SiAPD

Regarding to the two-color CMOS detector structure [196] and lateral n+/p+ in n-well photodetector architectures [197], a novel double-mixed APD structure has been proposed and implemented here. It is a Double-mixed Octagonal p+/p-sub and n+/p-sub with Active area= 50µm×100µm. The cross-section, layout and microphotograph of this APD (APD15) are shown in Figure 3.18. The measurement results on evaluation of this APD are listed in Table 3.10. This structure show a high-impedance and high-capacitance characteristics with a moderate gain and PDE in NIR region. The main advantage of this structure is offering a wide dynamic range and sensitivity to a wider range of light spectrum.



(a) (b) (c) (d)

Figure 3-17: The cross-section (a), the top view (b), the layout (c), and the microphotograph (d) of the fabricated APD15, in TSMC CMOS 180nm technology

Table 3.9: Main specifications of the Hybrid Octagonal n+p+/p-sub SiAPDs, fabricated using TSMC CMOS 180nm technology (Area=100×100 μm^2)

APD	Data source	Gain (M)	PDE @700nm	Impedance (Ω)	Capacitance	F @ M=17*	Breakdown Voltage (V)	DCR	Functional SiAPDs%
APD15	Simulation	150	**75%/71%**	900	5 pF	70/79	12	101Hz@Vex=1.7V	---
	Measurement	17±8	24±1%	930±4.27	9±0.10 pF	83±1	22±3.5	**117±1Hz@Vex=1.7V**	20
APD15+STI	Simulation	100	**55%/51%**	900	7 pF	70/79	12	**103kHz@Vex=1.7V**	---

*In 790nm. ** n+/p-sub APD structure with Shallow-Trench Isolation guard-ring.

3.9.6 Netted (Reticulated) SiAPDs

The "pinned" structure was first developed for CCD imagers [198] and subsequently reported for CMOS imagers as well [199]. Using this structure, in the same area, there are two pn junctions (the p+/n-well and the n-well/p-sub). This creates an effective depletion-region even larger than the n-well/p-sub diode which lead to a high collection-efficiency. However, depletion capacitances from the two junctions add in parallel, lowering the charge-to-voltage conversion. As the main source of dark-current is from the interface states at the surface of the junction, the high concentration of the free charge carrier at the interface, occupies the interface states and does not contribute to EHP-generation. Due to the high concentration of the holes in the p+ layer, this APD introduces a lower dark-current compare to the n-well/p-sub structure where the surface layer does not have a high free-carrier concentration [164], [188], [200]. Using the standard CMOS process, two types of p-n junctions have been implemented; one p+ /n-well junction and the other n-well/p-substrate junction. Using vertical p+/n-well junction eliminates the slow diffusion currents in the substrate region that limit high-speed operation. A novel structure is implemented using an array of small active areas covering a total rectangular area of 108µm×108µm. It is a net of p+/n-well SiAPDs (9×9 net) with different separation sizes: d=1µm (APD16) and d=5µm (APD17) shown in Figure 3.19. The APDs layout has been covered with metal-2 layer as a shield to block photons from reaching the substrate. Using this topology, a netted n+/p-sub SiAPD with n-well guard-ring is designed (APD18) as shown in Figure 3.19. The main characteristics of these new SiAPDs are listed in Table 3.11. This structure offered a low-noise characteristics compare to other structures. The APD16 and APD17 however didn't show sufficient gain and PDE characteristics. In APD18, a high-gain and PDE in NIR region with a low-noise behavior was observed. So this APD could be a proper candidate for low-noise and highly-sensitive photodetection applications. This APD also offers a low RC time-constant characteristics, makes it a good choice for high-speed photodetection applications as well.

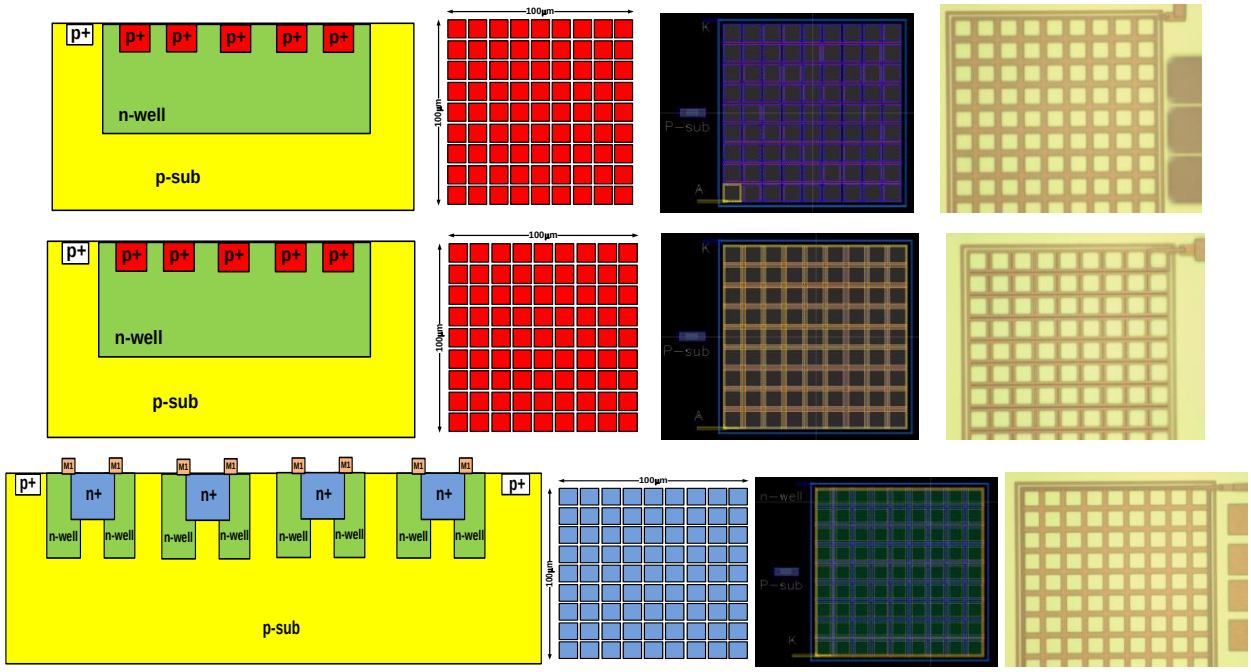


Figure 3-18: The cross-section (a), the top view (b), the layout (c), and the microphotograph (d) of the fabricated APD16 (first row), APD17 (second row), and APD18 (third row), in TSMC CMOS 180nm technology.

Table 3.10: Main specifications of the Netted (Reticulated) SiAPDs, fabricated using TSMC CMOS 180nm technology (Area=100×100 μm^2)

APD	Data source	Gain (M)	PDE @ 700nm	Impedance (Ω)	Capacitance	F @ M=3	Breakdown Voltage (V)	DCR	%Functional SiAPDs
APD16	Simulation	9	11%/11%	123	1 pF	61/59	91	99kHz@Vex=1.7V	---
	Measurement	5±4	4±1%	630±3.7	1±0.00 pF	83±1	112±20	**100±1kHz@Vex=1.7V**	16
APD16+STI	Simulation	9	**15%/11%**	118	1 pF	80/79	96	**140kHz@Vex=1.7V**	---
APD17	Simulation	3	**20%/18%**	0.5	1 pF	59/59	59	9kHz@Vex=1V	---
	Measurement	3±1	9±2%	0.8±0.18	1.3±0.1 pF	61±0.1	89±0.41	9±2kHz@Vex=1V	17
APD17+STI	Simulation	3	**20%/18%**	0.5	1 pF	50/59	59	11kHz@Vex=1V	---
APD18	Simulation	200	**65%/71%**	0.5	0.5 pF	36/40	16	24Hz@Vex=1V	---
	Measurement	**39±3**	60±5%	0.5±0.02	0.6±0.03 pF	**41±0.01**	19±2	30±4Hz@Vex=1V	91
APD18+STI	Simulation	184	**60%/67%**	0.5	0.5 pF	36/40	16	41kHz@Vex=1V	---

*In 790nm. ** n+/p-sub APD structure with Shallow-Trench Isolation guard-ring

3.9.7 Nested (Maze-Shape) SiAPDs

In order to offer a low-noise APD with high active-area, a new APD structure is developed in nested-shape as shown in Figure 3.20. Using this nested-shape, two different rectangular p+/n-well (APD19) and n+/n-well (APD20) SiAPDs have been implemented both with Active-area = 100µm×100µm. The evaluation results of these SiAPDs are listed in Table 3.12. Referring to the experimental results, this structure doesn't show high-gain and PDE characteristics compared to other structures.

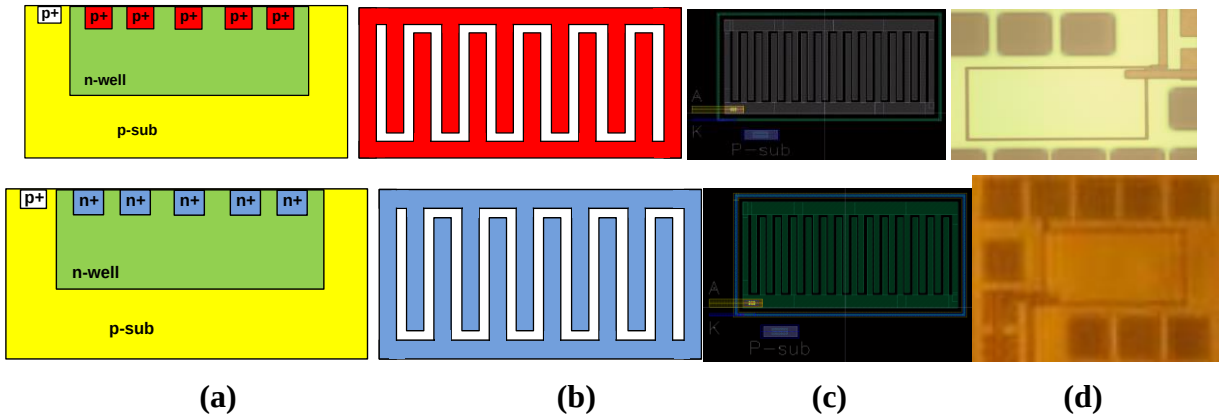


Figure 3-19: The cross-section (a), the top view (b), the layout (c), and the microphotograph (d) of the fabricated APD19 (first row) and APD20 (second row), in TSMC CMOS 180nm technology.

Table 3.11: Main specifications of the Nested (Maze-Shape) SiAPDs, fabricated using TSMC CMOS 180nm technology (Area=100×100 μm^2)

APD	Data source	Gain (M)	PDE @ 700nm	Impedance (Ω)	Capacitance	F @ M=9*	Breakdown Voltage (V)	DCR	%Functional SiAPDs
APD19	Simulation	10	**12%/12%**	600	1 pF	50/49	32	100kHz@Vex=1.7V	---
	Measurement	9±5	8±1%	630±3.7	1±0.00 pF	**53±0.1**	30±3.5	**100±1kHz@Vex=1.7V**	16
APD19+STI	Simulation	8	**25%/21%**	600	1 pF	60/59	41	140kHz@Vex=1.7V	---
APD20	Simulation	22	**20%/18%**	0.5	1 pF	80/89	29	0.5kHz@Vex=1V	---
	Measurement	11±4	18±2%	0.8±0.18	1.3±0.1 pF	**93±0.5**	37±3	1±1kHz@Vex=1V	79
APD20+STI	Simulation	17	**20%/18%**	0.5	1 pF	**100/98**	32	17kHz@Vex=1V	---

*In 790nm. ** n+/p-sub APD structure with Shallow-Trench Isolation guard-ring.

3.9.8 Quadratic SiAPDs

The p+/n-well and n+/p-sub SiAPDs have been implemented in quadratic topology shown in Figure 3.21. The APD21 is is a Quad -Rectangular net p+/n-well SiAPD with Active-area= 100µm×100µm. and the APD22 is a Quad -Rectangular net n+/p-sub SiAPD with Active-area= 100µm×100µm. These SiAPDs have been characterzised in Table 3.13. Using this topology, the n+/p-sub APD (APD22) has offered a higher gain and PDE characteristics with low-noise and higher functionality probability. So this APD could be applied for low-level light detection with higher SNR characteristics.

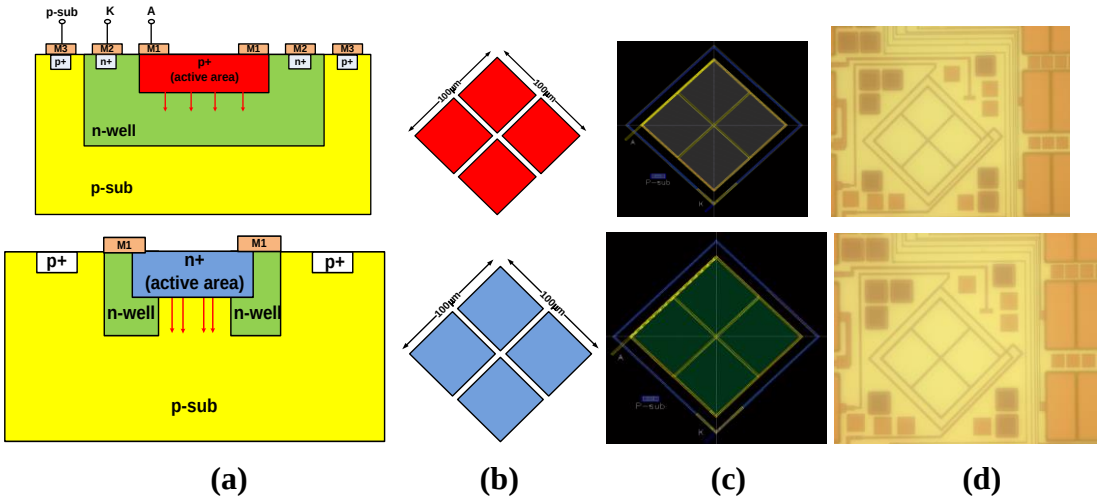


Figure 3-20: The cross-section (a), the top view (b), the layout (c), and the microphotograph (d) of the fabricated APD21 (first row) and APD22 (second row), in TSMC CMOS 180nm technology.

Table 3.12: Main specifications of the Quadratic SiAPDs, fabricated using TSMC CMOS 180nm technology (Area=100×100 μm^2)

APD	Data source	Gain (M)	PDE @ 700nm	Impedance (Ω)	Capacitance	F @ M=15*	Breakdown Voltage (V)	DCR	%Functional SiAPDs
APD21	Simulation	23	25%/21%	600	1 pF	69/68	33.5	100kHz@Vex=1.7V	---
	Measurement	15±6	16±4%	630±3.7	1±0.00 pF	73±1	52±3.5	108±1kHz@Vex=1.7V	83
APD21+STI	Simulation	23	25%/21%	600	1 pF	70/79	39	120kHz@Vex=1.7V	---
APD22	Simulation	70	60%/68%	0.5	1 pF	66/69	20	44kHz@Vex=1V	---
	Measurement	**36±11**	39±7%	0.8±0.18	1.3±0.1 pF	**65±0.2**	19±2	42±1kHz@Vex=1V	90
APD22+STI	Simulation	70	50%/58%	0.5	1 pF	70/59	20	45kHz@Vex=1V	---

*In 790nm. ** n+/p-sub APD structure with Shallow-Trench Isolation guard-ring.

3.9.9 Hexadecagonal SiAPDs

Circular shaped SPADs have better characteristics, due to sharp-edge prevention which reduces hot spots of electric field in corners creating PEB. However design rules prevented us from using circular geometries. So we already proposed and implemented different guard-rings to prevent PEB. But as an alternative, offering an APD with higher similarity to the circular-shape would probably offer a similar characteristics with less PDE and higher sensitivity. Here, as an alternative to prevent premature edge breakdown effect, a new technique is also proposed and implemented by shaping the SiAPD in a way to symmetrically distribute the corners around the active area as shown in Figure 3.22. Here we have implemented a hexadecagonal SiAPD using p+/n-well topology with Active-area= 100µm×100µm (APD23). Furthermore, a new SiAPD with

combination of guard-ring and this shaping technique is also implemented. This SiAPD is a n+/p-sub SiAPD with n-well guard-ring implemented in proposed hexadecagonal-shape with Active-area= 100µm×100µm (APD24). These SiAPDs have been characterized and the results are listed in Table 3.14. The results demonstrate that using this shaping-PEB technique offer a similar results as using guard-ring to prevent PEB. Combination of these two technique as well, it means using guard-ring in a shaping-PEB prevention design, as implemented in APD24, has offered the best APD in terms of gain, PDE, noise and functionality characteristics, compared to other implemented APDs.

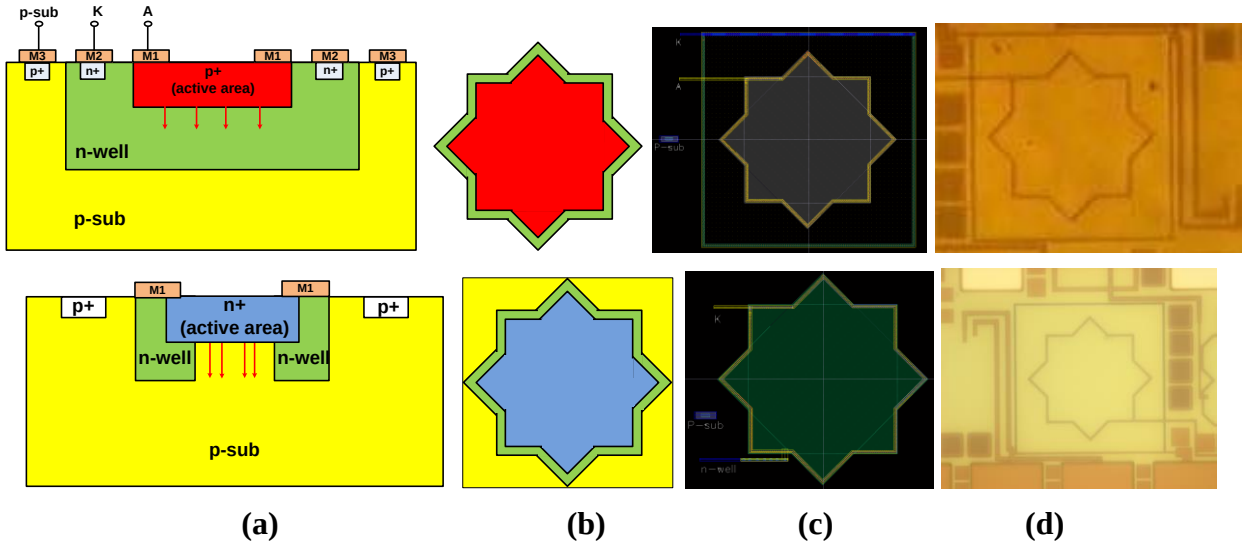


Figure 3-21: The cross-section (a), the top view (b), the layout (c), and the microphotograph (d) of the fabricated APD23 (first row) and APD24 (second row), in TSMC CMOS 180nm technology.

Table 3.13: Main specifications of the hexadecagonal SiAPDs, fabricated using TSMC CMOS 180nm technology (Area=100×100 μm^2)

APD	Data source	Gain (M)	PDE @ 700nm	Impedance (Ω)	Capacitance	F @ M=20	Breakdown Voltage (V)	DCR	%Functional SiAPDs
APD23	Simulation	115	75%/61%	600	1 pF	70/79	31	150kHz@Vex=1.7V	---
	Measurement	**30±10**	34±1%	630±3.7	1±0.00 pF	73±1	42±3.5	150±1kHz@Vex=1.7V	96
APD23+STI	Simulation	100	25%/21%	600	1 pF	90/89	32	194kHz@Vex=1.7V	---
APD24	Simulation	250	90%/98%	0.5	1 pF	85/79	9	64kHz@Vex=1V	---
	Measurement	**56±3**	70±2%	0.8±0.18	1.3±0.1 pF	86±1	11±1	64±1kHz@Vex=1V	97
APD24+STI	Simulation	210	90%/88%	0.5	1 pF	91/89	9	87kHz@Vex=1V	---

*In 790nm. ** n+/p-sub APD structure with Shallow-Trench Isolation guard-ring.

3.10 Comparison of the Implemented SiAPDs

Referring to the aforementioned simulation and measurement results on implemented SiAPDs in 180nm and 350nm CMOS technologies, we compared the achievements. Comparing the simulation and the measurements, a linear correlation was observed. However, a significant discrepancy was observed between simulation and measurement results especially in implemented SiAPDs in 350nm technology. The PDE and gain values were the highest observed discrepancies. The main sources of these differences, as they have been explained in this chapter before, are the inefficiency of the applied model, the pad's effects and the set-ups instrumentation. However in general the implemented APDs in 350nm technology didn't offer sufficient functionality especially in Geiger-mode operation, but the results confirms the impact of guard-rings on the functionality and quality improvement of the APDs in both 350nm and 180nm technologies. Comparing the implemented SiAPDs in 350nm CMOS technology, the rectangular APD with n-well guard-ring has offered better characteristics compared to other implemented APDs. The implemented n+/p-substrate, the n-well/p-substrate and the p+/n-well APD structures all can be used to detect visible, infrared, and NIR light, but with different performance regarding to the sensitivity, gain and noise characteristics introduced in this chapter. In general the n+/p-substrate structure offered a better performance compared to other ADP structures. The higher PDE of the n+/p-sub APD structure can be due to its ticker depletion-region on the p-substrate region with lower doping-concentration compared to the n-well or DNW region in p-well (d-tub) guard-ring APD structure.

Using STI has been considered only in simulations. It has added a significant noise to the device with a small improvement in gain and PDE (only in some cases). The introduced Hexadecagonal-SiAPD (APD24), double-Octagonal-SiAPD (APD14) and Netted-SiAPD (APD18), offer the best multiplication-gain and PDE charactersitics compared to other SiAPDs. The multiplication-gain of APD24, APD14 and APD18 are 56, 50, and 39, and their PDEs are 72%, 65% and 65% respectively. The introduced Hexadecagonal-SiAPD technique offers the highest functionality compared to all other techniques. The Hexadecagonal-SiAPD and Netted-SiAPD techniques however suffer from relatively poor (but acceptable) noise characteristics (high-F and DCR). The lowest breakdown voltages have been offered by Hexadecagonal-SiAPD (APD24) and p-sub

guard-ring (APD4 and APD5) techniques. The APD8, APD11 and APD18 offer low-impedance (0.52Ω) and APD15 offers a high-impedance (930Ω) device characteristics. APD11 and APD18 offer a low-capacitance (0.6 pF) while APD15 a high-capacitance (9 pF) device characteristics. The results demonstrated that using shaping-PEB technique offers a similar results as using guard-ring to prevent PEB. Combination of the guard-ring PEBP and shaping-PEB prevention techniques, as implemented in APD24, has offered the best APD in terms of gain, PDE, noise and functionality characteristics, compared to other implemented APDs.

3.11 Conclusion

In fNIRS, the Photoreceiver plays a critical role, affecting the efficiency of the whole system. Due to the low-level intensity of the light in fNIRS, the SiAPD is a proper candidate to be applied as photodetector. Developing SiAPDs using standard CMOS process offer a low-cost, low-power and fast implementation alternative. However it is limited by technology design roles. Here several SiAPDs have been implemented in novel structures and shapes (Rectangular, Octogonal, dual APDs, Nested, Netted, Quadratic and Hexadecagonal) using different premature edge-breakdown prevention techniques. The main characteristics of the SiAPDs have been validated and the impact of each parameter and the device simulator have been studied based on the simulation and measurement results in both 0.18µm and 0.35µm CMOS technologies. Implemented techniques exhibit SiAPDs with high avalanche-gain, low breakdown-voltage and high photon-detection efficiency accompanied with low dark-count rates. More details on the impact of premature edge-breakdown (PEB) and the PEB prevention techniques have been introduced in Appendix 2 by implementing 3 different p-sub, p-well, and n-well guard-rings using 180nm standard CMOS technology.

CHAPTER 4 DESIGN AND IMPLEMENTATION OF FRONT-END CIRCUITRIES FOR CW-FNIRS (LINEAR-MODE SIAPD FRONT-END)

4.1 Introduction

The bias of an APD just near but below a breakdown voltage is referred to as a linear-mode operation. At this bias voltage, the gain is high, and the output signal is proportional to the amount of scintillated light interacting in the APD. Based on the mode of operation, we need several amplifiers and processing blocks to operate the photodetector[126],[153],[90]. For linear-mode operation, SiAPD requires a transimpedance amplifier (TIA) to amplify and convert the input photocurrent into a voltage signal[201],[86],[202]. Transimpedance amplifiers (TIAs) are applied in photodetector front-ends of optical imaging systems such as pulse-oximeter, optical coherence tomography and functional near infra-red spectroscopy (fNIRS) as shown in Fig. 2.1. TIA performs a critical function to the rest of the front-end and plays a crucial role in determining many aspects of the overall performance of the receiver, including speed, sensitivity, and dynamic-range. Its design involves many trade-offs between noise, bandwidth, sensitivity, speed, power-consumption, transimpedance-gain and stability. This chapter addresses the design and application of the TIA in a fNIRS photoreceiver front-end. Different topologies are studied and characterized, then the most appropriate structures have been introduced. Three new TIA front-ends are proposed and implemented using standard submicron CMOS technology. The main objectives in design and implementation of these TIA front-ends were offering high gain-bandwidth product (GBW), low power-consumption, high transimpedance-gain, tunable bandwidth and low input and output noise characteristics.

4.2 Transimpedance Amplifiers

The most common amplifier architectures for low-power biomedical application include: three-opamp (TO) architecture[203],[204], switched-capacitor (SC) architectures [205] and Current-Balancing or Current-Feedback Amplifier (CBA or CFA) [206]. The CMRR of the TO amplifiers is highly dependent on the matching of the resistors. This matching requires laser trimming in standard CMOS technology that increases the cost. In addition, the necessity for low output-impedance opamps to drive the feedback resistors results in large power-dissipation. The SC

amplifiers are capable of eliminating the 1/f noise of the CMOS transistors, but they suffer from the noise fold-over above Nyquist frequency. To compensate this increase in noise, the power-dissipation of the SC amplifiers has to be increased. Therefore, SC architectures are not efficient for low-power and low-noise applications. The CBA topology eliminates not only the need for matched-resistors for achieving high-CMRR but also the need for low output-impedance amplifiers. Therefore, the CBA topology is convenient for implementing low-power and low-noise TIA and ideally suited for high-speed applications with moderate accuracy requirements. However, it is not appropriate for variable feedback resistor and capacitive inputs. Using chopper modulation[207] increases the CMRR and decreases the 1/f noise of CMOS transistor, but it suffers from inherent DC coupling. Using off-chip high-pass filters (HPFs) [207] also impose a very low input-impedance that degrades the SNR of the amplifier. Using a differential amplifier for introducing HPF characteristics to a chopper modulated amplifier[208] also consumes power due to the resistive-feedback topology [209].

Available photoreceiver front-ends include termination-resistor (low-impedance or high-impedance preamplifiers), and TIA (Fig.4.1(a)-(c)). The high-impedance receivers offer high-sensitivity and low-noise but they limit the dynamic-range and the bandwidth (need HPF and equalization) and lead to early saturation of the amplifier. The low-impedance receiver has high-BW, wide-dynamic range, used for transmission line matching and can be used with a variety of commercially available amplifiers with the cost of low-sensitivity and high-noise [210]. The TIAs offer high-BW, wide dynamic-range, high-sensitivity (controllable with feedback impedance) and a medium noise-level. Due to the adaptability of TIA with our application for low-power brain imaging, it was selected as the best option for this endeavor. Searching for a TIA which can be efficiently applied for LM-SiAPD operation, the main typical TIAs have been addressed include: the common-gate TIA (CG-TIA), resistive-feedback TIA (RF-TIA), and capacitive-feedback TIA (CF-TIA) shown in Figure 4.1(d)-(f). In resistive-feedback TIA (RF-TIA), the transimpedance-gain is high and offers the smallest noise especially at high frequencies compare to the other structures, but its BW is limited. Capacitive-feedback TIA (CF-TIA), offers a smaller noise at low frequencies but it is noisy at higher frequencies.

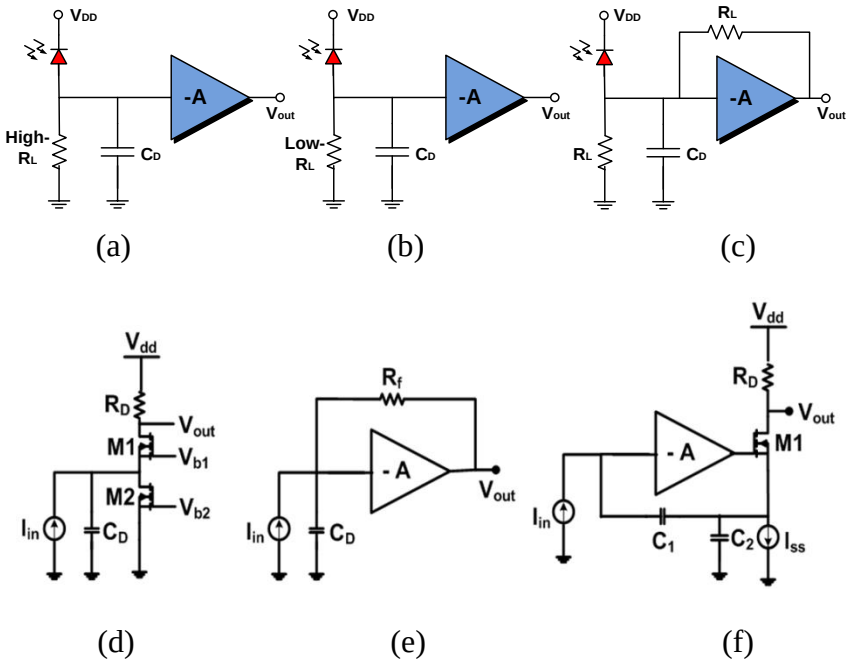


Figure 4-1: Typical Optical amplifier structures: (a) High-impedance, (b) Low-impedance termination-resistor, (c) transimpedance amplifier. (d) common-gate TIA, (e) resistive-feedback TIA, (f) capacitive-feedback TIA.

Common-gate TIA(CG-TIA), usually used in open-loop topology and exhibits low input-impedance and high transimpedance-gain, however its input noise current and input bias current are high and its BW is also low. A common-gate configuration is typically chosen as it can tolerate a wide-range of SiAPD capacitance. However, resistive-feedback architecture offers a better noise performance and is more attractive when SiAPD models are readily available [211]-[212]. Due to the low-level and usually high source impedance of input signals, the applied TIA should be established to meet certain basic requirements and must cope with various challenges in order to detect and extract the required signals. The challenges of designing such a TIA for portable biomedical imaging systems are: High Common-Mode Rejection-Ratio (CMRR) to reject the interference[213], High-Pass Filter (HPF) characteristics for filtering differential DC offset [214], Low-noise for high signal quality[215],[216], low power-dissipation (<50mW) for long-term power autonomy[217],[218], configurable gain and filter characteristics that suit the needs of different biopotential signals and different applications, high transimpedance-gain (>1k) [219], [220], narrow Bandwidth (around 100k), high output-swing, wide dynamic-range, ambient-light rejection, and low-voltage operation [120].

Besides so much works [14]-[30] on developing a proper photoreceiver amplifier, designing such a proper dedicated front-end for fNIRS has not been considered in the literature yet and none of the reported NIRS detectors provide these features taken together, which is a crucial factor in real-time brain imaging. Available proposed amplifiers for this case are suffering from several limitations so that trade-off between necessary parameters occurs with the cost of losing reliability and performance. For example reported variable-gain transimpedance amplifiers are difficult to stabilize [209]. The key problem with these designs is that they are based on the traditional two-stage topology consisting of a common-source gain stage followed by an output buffer. Phang et. al. [120] proposed a TIA combining a sub 1-V current mirror and a common-gate TIA based on a current-gain amplifier for optical communication. Achigui et. al. [221] modified this TIA by adding an Operational Transconductance Amplifier (OTA) with dynamic threshold transistor (DTMOS) for NIRS front-end photoreceiver. All of these designs are based on fixed-gain and only one mode of operation. Reaching high data-rate and high-BW in these designs is also with the cost of small gain, high noise and power-consumption. So the needs for a new design with the ability to overcome these limitations and cover the requirements for a fNIRS photodetector front-end, is a critical issue which is addressed in this chapter.

4.3 Implemented TIAs

Here we have proposed and implemented three new TIAs. The main specifications of these TIAs are explained in detail in follow.

4.3.1 The First TIA circuit (TIA1)

Using distributed gain amplification and adaptive feedback it is possible to change the gain of the amplifier without varying the BW. We have used this fact in order to make the intensity of the photoreceiver independent to the BW variation. This is the technique applied in many organic photoreceivers [222], [223], [224], [225]. By considering the distributed-gain (multi-stage amplification) concept in TIA design [217] we have proposed the configurations shown in Figure 4.2(a). Using distributed-gain concept in TIA design also increase the gain-bandwidth product (GBW) of the circuit [226]. Because of the inverse dependency of gain and BW in a single-stage amplifier, designing a single-stage amplifier with high-GBW is not easy. A cascade amplifier has

a significantly larger GBW than a single-stage amplifier with the same gain. If the GBW of each amplifying stage is constant, then the time-constant for an N-stage amplifier with identical gains per stage is proportional to $\sqrt{\mathrm{N}}$. $\sqrt[\mathrm{N}]{\mathrm{A}}$ versus being proportional to A for the single-stage case [217], [226], [227].

The core design consists of a current amplifier implemented in a transimpedance configuration. It is a combination of CG-TIA and RF-TIA architectures implemented in [150], [201]. Here we have used dynamic-threshold voltage MOSFET (DTMOS) in order to enhance the differential input common-mode range (ICMR). In this circuit (Figure 4.2(a): TIA1), the M1-M5 and M8 constitute the current amplifier introduced in [167]. The common-gate transistor M1 sets the input voltage to $V_{bias1} - V_{gs1}$ which is adjustable to keep the M4 transistor in active region. The TIA output is biased at V_{gs5} which can swing down to $V_{ds,sat3}$. This offer a wide output swing up to the threshold voltage. The combination of three transistors (M6, M7 and M9) has been simply used to work as a feedback resistor to minimize the output ripple and omit the extra drawn-current. The DC transimpedance-gain is given by:

$$\frac{V_{out}}{I_{in}} = -\frac{g_{M5}R_f - 1}{g_{M4} + g_{M5}}. \tag{4.1}$$

where g_{M4} and g_{M5} are the transconductance of transistors M4, M5, and Rf is the feedback resistance implemented by M6, M7 and M9 biased in the linear region. The closed-loop bandwidth of the TIA is approximately equal to the unity-gain frequency:

$$BW \approx \frac{1+A}{R_f C_D} \approx \frac{A}{R_f C_D} \approx \omega_t. \tag{4.2}$$

$$\omega_t \approx \frac{A}{R_f C_D} \approx \frac{g_{m1}R_1}{R_f C_D}. \tag{4.3}$$

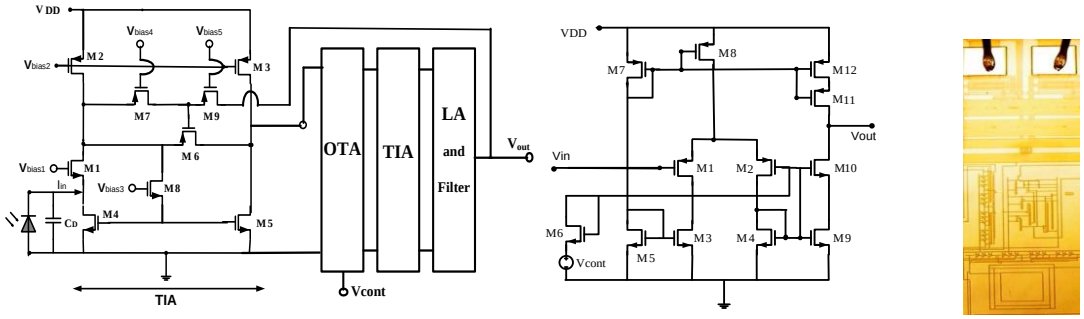
where $\mathrm{C_D}$ is the APD capacitance and ω_t is the frequency where the loop-gain of the TIA is unity. The bandwidth of the TIA increases by decreasing the $\mathrm{C_D}$. We have used the $\mathrm{C_D}$=1pF in simulations as this is the commonly reported value [9],[228]. In order to boost the voltage-swing and match the output impedance to drive the photoreceiver output (usually a counter or an analog-to-digital converter), a Limiting Amplifier (LA) [229] and a current-mirror Operational Transconductance Amplifier (OTA) [221] are used at the output of the TIA. The LA circuit is

implemented by cascading two stages of resistive-load differential amplifiers and one stage of buffer. The OTA preamplifier is used to selectively amplify the low-amplitude signal before it is being filtered and then demodulated. This current-mirror OTA, is modified from OTA reported in [221]. Performance of this OTA which is shown in Fig. 4.2 (b) is highly dependent on the bias current (I_{bias}), and the sizing of the transistors. We have considered these two parameters fairly in order to reach the best performance. The OTA differential input pairs are in a class AB configuration, and uses DTMOS devices for input common-mode range enhancement. Furthermore both the OTA and the TIA have low-pass response individually, but when output TIA and OTA together, OTA will have a high-pass response and helps towards offering a more tuneable circuit. To increase the maximum output swing, and improve the stability of the circuit, we have also used a filtering block followed by TIA and LA. Because one of the main requirements of biosignal amplifiers is to have a wide dynamic-range, here in order to achieve wide dynamic-range, we have considered the proposed photoreceiver circuit by adding the ability of parameters tuning. Using the constant applied voltage of $V_{cont}(0V < V_{cont} < 2V)$, the Gain, BW, power-consumption and dynamic-range of the output could be changed in a wide desirable output range.

We used CADENCE schematic editor and Virtuoso layout editor to design and simulate our proposed TIA in 0.35µm CMOS technology. In order to optimize the performance of the amplifier, we analyzed the sensitivity of each circuit component on the output and the best values for optimal sizing were selected. The simulation and measurement results of the proposed circuit verifies its efficiency and reliability for fNIRS system. For TIA:$Z_{in,dc} = 500\ k\Omega, V_{in,dc} = 0.5\ V$ and for the total front-end: $Z_{in,dc} = 300\ \Omega$, $V_{in,dc} = 3\ mV$. We need low input-noise for high signal quality. Due to the low-frequency behavior of the signals, in-band noise of the readout is dominated by 1/f noise. The implemented TIA shows a low-level input-noise characteristic. This shows the efficiency of the applied topology and using DTMOS accompanied with optimal transistor scalling based on the sensitivity analysis. The main characteristics of this TIA are summarized in Table 4.1. Figs. 4.3 (a)-(c) show the transimpedance-gain, the input and output noise of the implemented circuit as function of frequency variation. By varying the V_{cont} in proposed variable-gain front-end between 0-1.5 V, we reached the very-high and fixed value of 45×10^9 for gain-bandwidth product (GBW). This value is tuneable between 10M-45G for

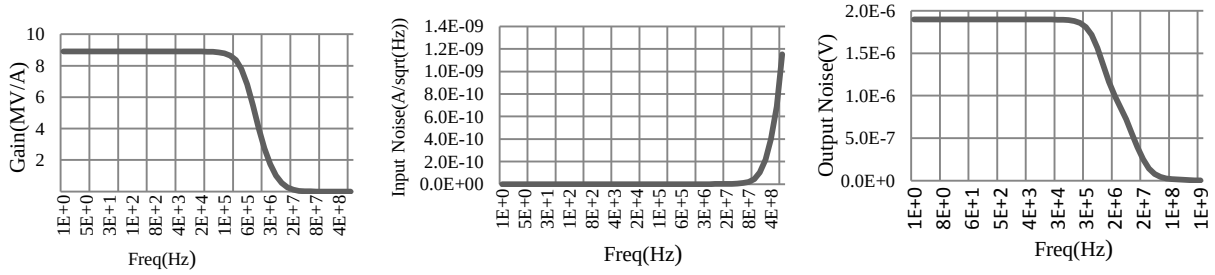
various applications. We reached the transimpedance-gain in the range of 2-400 MV/A and BW in the range of 1.7-5MHz using this configuration. The power-consumption of this circuit is in the range of 0 - 3.5 mW, which is very convenient for biomedical wireless and portable applications. Referring to the Table 4.1, the input-noise of the implemented TIA is one of the lowest reported input-noises comparing to other similar photoreceiver amplifiers. The output pulse with the maximum swing of 3.3V is also one of the best indexes to show the appropriateness of the proposed design. In order to verify the effect of the supply-voltage, we have also tested the tuneable-gain configuration by decreasing the supply-voltage, down to 1V. In order to validate the robustness of the circuit performance against power-supply variation we have examined the TIA front-end characteristics for the supply voltages vary between 1 - 3.3V.

For more detail about this TIA, refer to the Appendix 3 and [166], [175], [9], [117].



(a) (b) (c)

Figure 4-2: Schematic diagram of the implemented tuneable distributed-gain TIA (a) and the OTA (b). The microphotograph of the fabricated IC using TSMC CMOS 350nm technology (c).



(a) (b) (c)

Figure 4-3: The gain (a), the input noise (b) and the output noise (c) of the implemented circuit

4.3.2 The Second TIA circuit (TIA2)

A single-stage amplifier is not sufficient to offer a high-Gain, high-GBW, and fast (high-bitrate) TIA characteristics. So here we have implemented the four-stage TIA (TIA2) structure shown in Figure 4.4 [86]. In order to avoid extra biasing circuitry, no biasing point has been considered in this design. The circuit consists of an inverter string (M1-M2, M4-M5, M7-M8). Each inverter block is followed by a transistor (M3, M6, M9) used as a diode for self-adjusting bias and driving the next block. A resistive-feedback configuration is used due to its better noise characteristics. This configuration is also useful in case the APD model be readily available. For cascade TIA in order to reduce the relative noise contribution of the subsequent amplifier stages, the signal-to-noise-ratio (SNR) of the first stage should be tuned to be as large as possible so the feedback transistor (Mf) is placed in series with Rf to reduce the input-noise of the TIA by applying different control voltage via Vcont. The amplifier blocks 2-4 are the same as the first depicted block is. Using 4-stage amplification technique, distribute the overall gain and lead to a higher gain-BW product (GBW) value. The DC gain of a single stage is equal to:

$$A_i = \frac{g_{m1}+g_{m2}}{g_{m3}+g_{ds1}+g_{ds2}+g_{ds3}} \approx \frac{g_{m1}+g_{m2}}{g_{m3}} \qquad (4.4)$$

And the BW is calculated by:

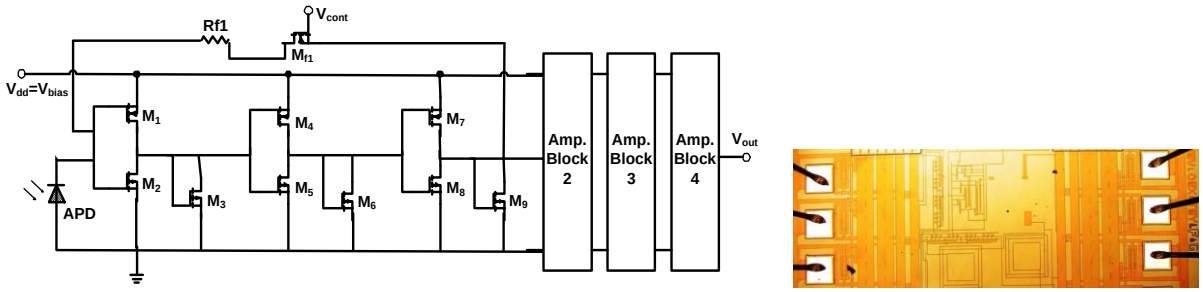
$$\mathrm{BW} = \frac{1+\mathrm{A_i}}{2\pi \mathrm{RC}} \qquad (4.5)$$

where A is the gain and C is the input capacitance of each stage. The equivalent thermal noise of each stage is equal to:

$$\mathrm{di}_{\mathrm{in}}^2 = \frac{4}{3}\frac{\mathrm{KTA}^2}{\mathrm{g_m R}^2} \qquad (4.6)$$

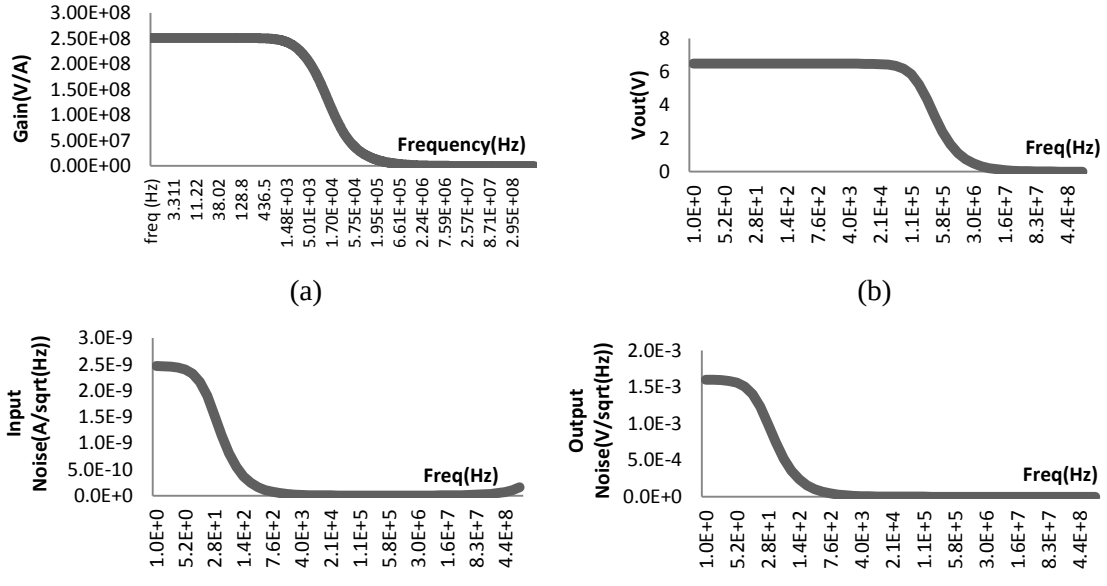
In order to offer a better performance we have selected the $\frac{\mathrm{W}}{\mathrm{L}}$ for M2,M2,M4,M5,M7, M8 high and for M3,M6 and M9 low. The $\frac{\mathrm{W_2}}{\mathrm{W_1}}, \frac{\mathrm{W_5}}{\mathrm{W_4}}, \text{and } \frac{\mathrm{W_8}}{\mathrm{W_7}}$ are also considered high. To reach the best performance design, the sensitivity of each component presented in this circuit has been analyzed and the best scales for optimal sizing are selected. This TIA front-end has been fabricated using CMOS 0.35 µm technology. The layout of the fabricated IC is shown in Figure 4.5(b). The TIA gain and its frequency response are depicted in Figs. 4.5 (a)-(b). The input and output noises are shown in Figs. 4.5 (c)-(d). At Table 4.1 the characteristics of this TIA have been compared with

other currently proposed works. The transimpedance gain of the proposed circuit is tunable between 10KV/A-250MV/A and its BW is also tunable from DC to 100KHz and 1MHz by varying the control voltage (V_{cont}) and based on the frequency of the noise. The total power-consumption is 4mW. The input noise is 200fA/√Hz at 1kHz and the maximum output-swing is 3V. For more detail about this TIA, refer to [68], [65], [39].



(a) (b)

Figure 4-4: The schematic of the implemented optoreceiver amplifier: TIA2 (a), and the microphotograph of the fabricated TIA using TSMC CMOS 350nm technology (b). Here $M_1, M_4, M_7: W/L = 2.5/0.35,\ M_2, M_5, M_8: W/L = 10/0.35$ and for all other transistors $W/L = 1/0.35$.



(a) (b)

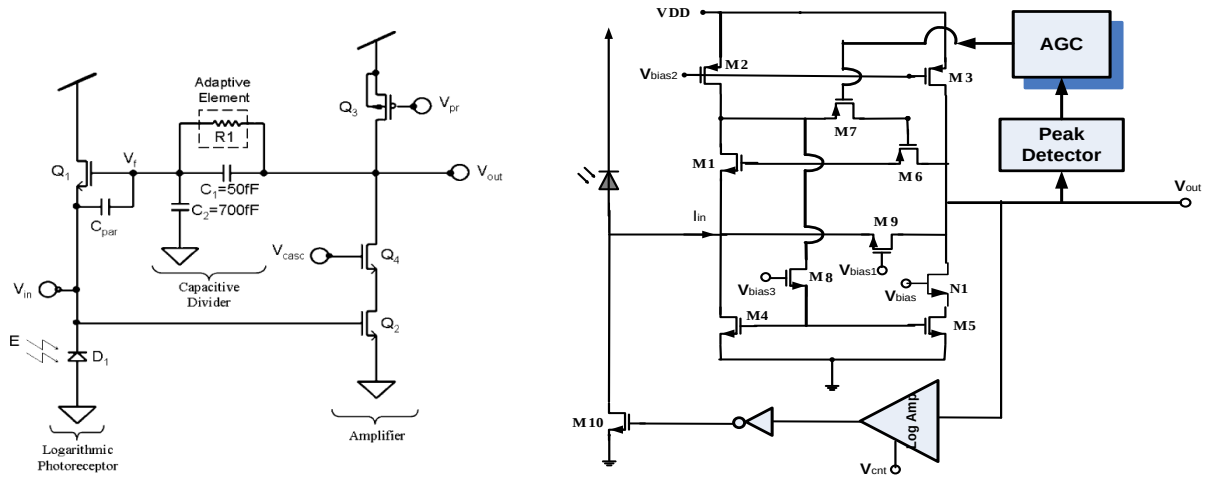
(c) (d)

Figure 4-5: The TIA gain (a), Frequency-response of the output voltage (b), the input-noise (c) and the output-noise (d).

4.3.3 Logarithmic TIA (LogTIA)

A Logarithmic Transimpedance Amplifier (LogTIA, TIA3) is implemented with Automatic Gain-Control (AGC) and Ambient-Light Rejection for low-level light detection applications [230]. The LogTIA provides a wide dynamic-range operation with a moderate power-supply voltage. The minimum detectable contrast in a LogTIA is not dependant on the input-current intensity, because the BW and therefore integration interval of the system scales with input-current so that a constant number of the electrons are always gathered during the sensing period [231]. In linear-TIA, the BW and subsequently the integration intervals of the system are fixed such that the minimum detectable contrast is worsened at low-input intensities due to the gathering of the more electrons [231], [217]. The LogTIA can be considered as a linear-TIA with a built-in gain controller, such that the feedback resistance (R_f) varies with input-current (I_{in}) to keep the $I_{in} \times R_f$ fixed. The circuit schematic of a well-known logarithmic transimpedance photoreceptor is shown in Fig. 4.6(a) [232]. C1, C2 and R1 in Fig. 4.6(a) form a temporal low-pass (LP) filter in the feedback path, which results in an overall high-pass (HP) characteristic for the photoreceptor and boosts the gain for ac signals (beyond the HP pole frequency) [232]. The output voltage of this photoreceptor is equal to:

$$v_{out} = \left(\frac{KT}{q\kappa_s}\right)\left(\frac{C_1+C_2}{C_1}\right) \times \left(\frac{i_{ac,in}}{I_{DC,in}}\right) \qquad (4.7)$$



(a) (b)

Figure 4-6: (a) Circuit schematic of a state-of-the-art logarithmic transimpedance photoreceptor, (b) Introduced logarithmic TIA (TIA3) with ambient light rejection and AGC loops

The drawback of this circuit is that the limited gain of the amplifier and the effect of the parasitic capacitances (Cpar) limit its light-sensitivity and decrease its speed and BW. Applying an automatic gain control and DC rejection feedback can increase the sensitivity and BW. LogTIA is practically useful in systems that need scale-invariant and wide dynamic-range operation [231], [217]. Its sensitivity to the contrast (ac/dc) of the input and its scale-invariant fractional amplification is beneficial in several applications where percentage changes rather than absolute changes carry information. This photoreceptor was inspired by the operation of biological photoreceptors in turtle cones and bears many of its properties including higher ac gain than dc gain, a contrast-sensitive response, and a relatively wide dynamic-range of operation [233]. Unfortunately, the merit characteristics of this amplifier especially for biomedical imaging and optoelectronic circuits and systems are not introduced well and only limited applications of LogTIA in photodetector implementation have been reported. The previously reported applications of logarithmic TIA in the photodetectors are limited to the works presented in [231], [217], [222]. A LogTIA is also implemented in [231] for pulse-oximetry application. But no application of LogTIA for fNIRS system has been reported yet in the literatures. The unique characteristics of LogTIA have been introduced as a state-of-the-art front-end circuit for photodetection especially in near infra-red region of light spectrum and a new LogTIA has been introduced and implemented to be applied in functional near infra-red spectroscopy (fNIRS) photodetector front-end. This is the first introduced and successfully designed and implemented application of LogTIA in a near infra-red photodetector front-end and in fNIRS application.

In this circuit (Figure 4.6(b)), the main TIA core is the same as TIA1 (introduced above) which is modified to work as logarithmic amplifier. Here the M1 act as the logarithmic amplifier transistor, M6-M7 provide the feedback resistor. M9 acts as a feedback transistor placed directly across the input and output terminals of the current mirror. Using this direct feedback topology, decrease the input impedance seen by the photodiode and improve the speed of the circuit, with the cost of a lower output-swing. Using a logarithmic amplifier makes the response to a fixed image contrast invariant to absolute light intensity and improves the dynamic-range of the photodetector. The N1 transistor at the output of TIA, cause the circuit acts as a cascade current mirror, reduce the output voltage variation by boosting the output impedance and reduce the v_{DS} -mismatch effect. Using an automatic gain control and DC rejection feedback we have increased the sensitivity and BW. The transimpedance gain of the linear TIA increases the sensing speed by

decreasing the time constant such that the rapid changes in the input are not filtered at the output. The input voltage (V_{in}) is kept at a virtual reference value (V_{ref}) by the feedback loop such hat it doesn't change by the variation of the input current, thus the current variations due to the Vin variation (e.g. due to early effects and other sensor effects), are minimized. By increasing the power-supply, the dynamic-range of the output-voltage can be maximized, while maintaining the APD breakdown-voltage at the input. In contrast, the logarithmic TIA, uses a sub-threshold transistor as the feedback element with an exponential parameter of κ_s (the sub-threshold exponential coefficient of M_f) and a pre-exponential constant of I_{os}. The key motivation for using the logarithmic instead of linear sensing is that it is inherently sensitive to the contrast (ac/dc) of the input photocurrent signal. By assuming V_{ref} and considering that the i_{in} and v_{out} are the small changes in the operating-point current (I_{IN}) and voltage (V_{out}) respectively, the output voltage of the LogTIA is equal to:

$$v_{out}(s) = \frac{KT}{q}\left(\frac{i_{in}}{I_{IN}}\right)\left(\frac{A/(1+A)}{1+\frac{s(C_{in}/g_f)}{1+A}}\right) = \frac{KT}{q}\left(\frac{\Delta I_{IN}}{I_{IN}}\right)\left(\frac{A/(1+A)}{1+\frac{s(C_{in}/g_f)}{1+A}}\right) = V_{ref} + \frac{KT}{q\kappa_s} ln\left(\frac{I_{in}}{I_{Ios}}\right)$$
$$v_{out} = \left(\frac{dV_{out}}{dI_{in}}\right) i_{in} = \left(\frac{KT}{q\kappa_s} \times \frac{1/I_{Ios}}{I_{in}/I_{Ios}}\right) i_{in} = \left(\frac{KT}{q\kappa_s}\right) \times \left(\frac{i_{in}}{I_{in}}\right) = \left(\frac{KT}{q\kappa_s}\right) \times \left(\frac{i_{ac,in}}{I_{DC,in}}\right) \quad (4.8)$$

In order to keep the photodetector gain stable under temperature and ambient-light variations we develop an automatic gain monitoring and control (AGC) mechanism and an ambient light rejection circuit (include LogAmp, buffer and M10) on the implemented TIA circuit that also increased the input dynamic-range. The detail of the applied ambient-light rejection circuit is presented in [67]. The applied peak-detector circuit also has been explained in [217] and [231]. The general characteristics of the implemented LogTIA (TIA3) are shown in Table 4.1. For more details about this TIA, refer to [150], [217], [230], and [231].

Integrated Photoreceiver Front-End

The proposed TIA front-ends have been implemented using standard CMOS 0.35µm technology, fabricated by TSMC via CMC Microsystems, and their general characteristics are shown at Table 4.1 compared with other works. The implemented TIA front-ends offer high gain-bandwidth product (GBW), low power-consumption, high transimpedance-gain, tunable bandwidth and low

input and output noise characteristics. Using the constant applied voltage of $V_{cont}(0V < V_{cont} < 2V)$, the Gain, BW, power-consumption and dynamic-range of the output could be changed in a wide desirable output range. TIA1 offers very low-power consumption (0.8 mW) and an ultra-low input current noise. TIA2 can be applied in a wide BW range (100kHz - 1MHz) with low-noise and power. The TIA3 has been implemented in 2 different CMOS technologies. Using AGC and noise rejection in LogTIA (TIA3) have reduced the input current noise (with factor of 0.1) and have increased the GBW (with factor of 6.8) compare to the regular LogTIA.

Table 4.1: General characteristics of the proposed and implemented TIAs

Ref.		Tech.	Supply voltage (V)	Power diss. (mW)	Max Gain	BW (MHz)	Input Noise at 1kHz (A/√Hz)	Max. Swing (V)	F.O.M	Control
[234]		0.8	8	-	150k	120	1p	-	-	No
[119]		0.35	3.3	-	17.78k	70	-	-	-	Gain, BW
[115]		0.6	3	30	8.7 k	500	4.5p	-	145	No
[120]		0.35	1	1	210k	50	11 p	1	10500	No
[235]		0.18	2	19.5	12.6 k	2400	19p	-	1549	No
[236]		0.18	2	170	22.4 k	7600	-	-	1001	No
[229]		0.5	5	-	4 k	374	-	80m	-	No
[237]		0.18	2	70.2	1.12 k	7200	8.2p	-	115	No
[221]		0.18	1	0.018	2.2 k	0.4	-	0.7	48.9	No
[238]		0.18 BiCMOS	2	10.7	1.58 k	2000	4.2p	-	296	No
[239]		0.35	3.3	17	1.778k	1900	9.7p	-	198.72	No
[109]		0.5	5	53	398	532	22p	-	3.995	Gain, BW
[240]		0.13	1.5	98	1.3 k	6000	-	-	79.59	No
[241]		0.13	1.5	47	1 G	5950	-	-	125532	No
[242]		0.18	1.8	33.3	245	10500	-	-	77.252	BW
[243]		0.35	3.3	53.5	501	2750	12.76p	-	25.752	No
[244]		0.35	2.5	0.14	1.49 k	110Hz	-	-	0.001	BW
[245]		0.25	3.3	185	-	1744	-	3	-	Gain
[246]		0.18	2	7.2	6.3 k	2500	<10p	-	2190	Gain, BW
TIA1	TIA	0.35	3	3.5	250G	0.151	112 f	3	10785714	Gain, BW
	TIA+LA	0.35	2	2	250 k	11.5	44.86 p	2	1437.5	Gain, BW, Power
	TIA+OTA +TIA+LA	0.35	1	1.5	90 M	0.072	59 f	1	4320	Gain,BW,Power
			3	0.8	400M	1000	1f	3	500M	Gain,BW,Power
TIA2		0.35	3	4	250M	1	200f	3	62500	Gain, BW
TIA3		0.35	3	0.2	300M	2000	50f	3	3K	Gain,BW,Power

*FOM= $\frac{G \times BW}{(Power\ dissipation) \times Noise}$ [GHzΩ/mW]

4.4 Multi-Building Blocks Integration (APD and TIA)

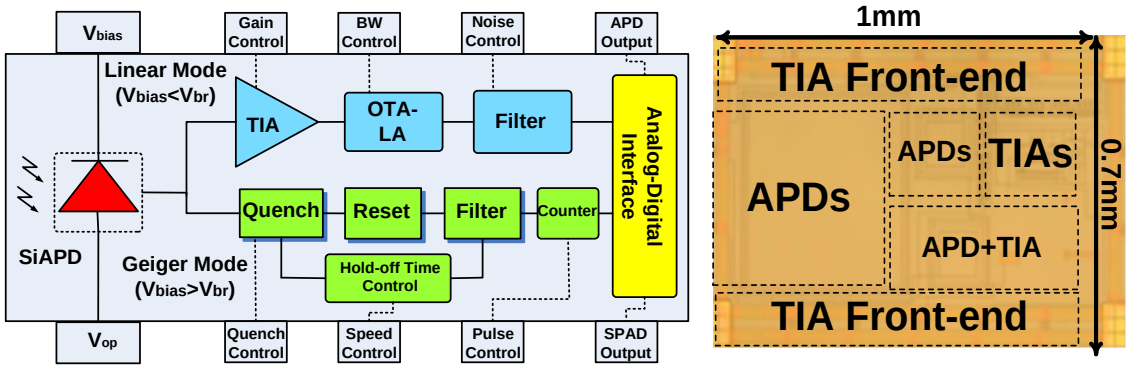
Chip-level integration provides higher performance with less required system components, less power-density and power-consumption. Integration offers more reliable and lower-cost systems that are easier to manufacture and maintain. It reduces the design complexity by offering lower communication latency and eliminating generalized transactional interfaces that are typically used when modules communicate across chip boundaries. To increase the use of photodetector systems for state-of-the-art biomedical applications, integration of the SiAPD and the high-speed peripheral circuitry on the same chip using standard CMOS technology is highly desired. Several research groups have fabricated SiAPDs using standard CMOS technology and also integrated the APD with TIA front-end. Although due to their relatively high-power consumption and low sensitivity and SNR characteristics their performance is still far from the one obtained with commercial APDs.

Here we have integrated the proposed SiAPDs and TIA front-ends on the same chip (Figure 4.7) and the measurement results regarding to this integration are shown in Table 4.2. In order to design a continuous-wave fNIRS photodetector front-end, an amplifier front-end is developed [87] in order to be integrated with the SiAPD in the same chip. The goal was to develop a compact and cost-effective photodiode and other electronic circuits of a NIRS front-end receiver on the same chip using standard CMOS process. The final layout of the designed integrated circuit after post-layout simulation and optimization was fabricated by TSMC via CMC Microsystems. The fabricated IC includes individual APDs and TIAs and also the on-chip integrated APD+TIA on the same die. The on-chip integrated APD+TIA has been characterized and the effect of on-chip APD and TIA integration has been investigated by comparing the characteristics of this on-chip APD+TIA with the individual interconnected APD and TIA from different ICs (same die).

The measurements were established on-wafer and using Air-Coplanar Probes. The wafer probes were calibrated using the Line-Reflect-Match calibration method for S-parameter measurement. The complete four-port S-parameters for the TIA were measured using on wafer probing with an HP8510 two-port vector network analyzer. Each of the measurements was taken over a frequency span of 1Hz to 5GHz with a total of 400 points. The sensitivity, SNR, noise, gain and power consumption for each CMOS-APD separately and for the integrated photoreceiver (APD+TIA)

are measured and compared in Figure 4.8. In order to verify the impact of the applied APD structure and size on these different measured values, this comparison has been established for different APDs.

Referring to the Figures 4.8 and 4.9, a regular variation is observed in each examined parameter for all APDs. Except a reduction in sensitivity of the rectangular APD2 (which can be due to the BW and thermal noise degradation in this structure introduced by integration), for all other integrated APD structures a significant improvement in sensitivity, SNR, noise and scale is observed in integrated circuit with the cost of higher power-consumption. No significant change is observed on the multiplication gain and BW. Furthermore, the impact of integration is mainly on SNR and then on the power, sensitivity and noise respectively. In addition to the photon-detection efficiency and dark-count rate that limit the minimum detectable power, the dynamic-range (DR) which is define as the ratio between the maximum and minimum detectable power is also an important parameter that is 80dB and 92dB for APD1 and APD2 respectively. The implemented TIA front-ends (Table 4.2) offer the highest transimpedance gain and the lowest power-consumption and input/output noises accompanied with a suitable gained performance regarding to the APD+TIA on-chip integration. In Fig. 4.9 (a) the dark current noise of the CMOS integrated photoreceiver and CMOS-APD only when Vr = 9V and incident optical power = 0 dBm are compared. While the photodetection frequency response (PFR) for the proposed APDs is not high, the integration has improved the PFR significantly. As the reverse bias voltage is increased, the photodetection frequency response increases because of increased avalanche gain. Optimization of the CMOS-APD utilizing RF-peaking can enhance photodetection 3-dB bandwidth while maintaining sufficient avalanche gain. The maximum 3-dB bandwidths for the integrated circuit of APD1+TIA and APD2+TIA are around 3.79 GHz and 2.78 GHz respectively at the reverse bias voltage of 10.6V. Integrated circuit specially regarding to the square APD2 has better BW performance than APD1. However integration has no significant effect on the gain of TIA but reduces the input referred current noise as depicted in Fig. 4.9 (b)-(c). As shown in Table 4.2, comparing with other works, the implemented integrated circuit shows lower power-consumption and noise and higher sensitivity while offering no significant improvement in data-rate. However the acceptable data-rate of the proposed circuit has no significant preference over other works but more works is still on progress in order to increase the speed of the photodetector front-end.

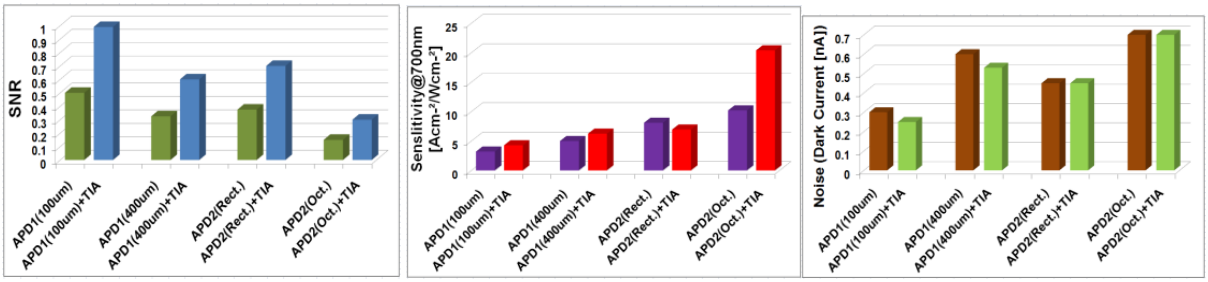


(a) **(b)**

Figure 4-7: Block diagram of proposed front-end photoreceiver IC working in linear and Geiger mode (a), and the microphotograph of the fabricated IC using TSMC CMOS 350nm technology (b).

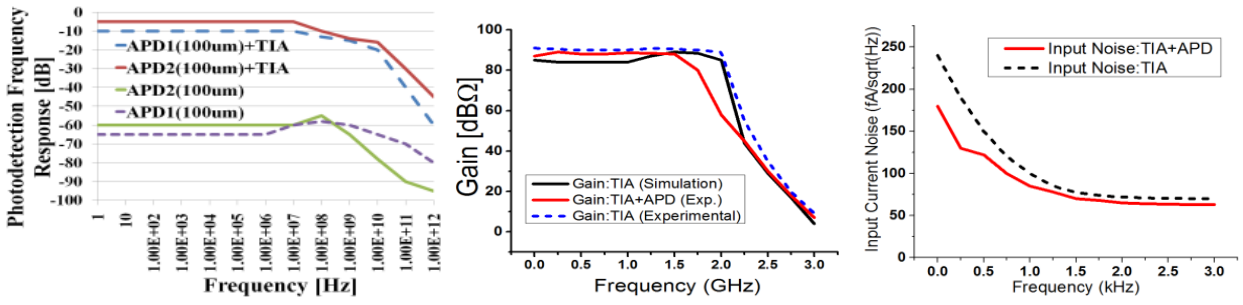
Table 4.2: The general characteristics of the implemented integrated SiAPDs with TIA

Circuit / Parameter	TIA+APD1		TIA+APD2		[247]	[248]
	Rectang	Rectang.	Rectang.	Octag.		
CMOS Tech.(µm)	0.35	0.35	0.35	0.35	0.18	0.13
SupplyVoltage(V)	3 V	3 V	3 V	3 V	1.8	1.3
APD Gain (M)	20	100	45	15	-	-
APD Area (µm)	100×100	400×400	100×100	100×100	-	-
Sensitivity (dBm)	-4.3	-2.2	-6	-22	-19	-5.5
Vbr (V)	9	9	6	6	-	-
Power diss. (mW)	5.12	2.31	0.91	1.16	50	21.6
Max TIA Gain	249M	245.01M	248.6M	248M	-	
BW (MHz)	1200	1643	1420	1006	-	-
Data Rate (Gb/s)	5.68	3.31	4.17	2.4	3	4.25
Log(BER)	-13	-13	-12	-11	-11	-12



(a) (b) (c)

Figure 4-8: Comparison the impact of integration on different parameters: the impact of integration on SNR (a), Sensitivity (b), and the dark-current noise (c).



(a) **(b)** **(c)**

Figure 4-9: Comparison of the PFR (a), gain (b) and input-current noise (c) characteristics of the integrated and individual TIA front-ends.

4.5 Conclusion

The main challenges to design an efficient TIA for biomedical imaging applications were addressed in this chapter following by introducing 3 new miniaturized, reconfigurable and low-noise photodetector front-ends implemented on-chip using standard CMOS technology. The implemented TIA front-ends offer high gain-bandwidth product (GBW), low-power consumption (<1mW), high transimpedance-gain (up to 200MV/A), tunable bandwidth (0.1kHz-1GHz) and low input and output noise (~few fA/√Hz and few μV/√Hz). These characteristics make them a proper candidate to be applied for detection of low-level bio-signals such as in fNIRS and EEG and will drive a great expansion in their application for low-power and low-noise wireless biomedical imaging applications. The main effects of on-chip integration of APD and TIA front-end have been also addressed. The on-chip integrated APDs with the proposed TIA preserved the high-performance characteristics of both APDs and TIA while offering a more miniaturized photodetector front-end dedicated to low-intensity light detection applications. The integration improved the SNR, sensitivity, fill factor (FF) and PFR with no significant change in power and gain values. Using APDs with larger active areas and applying p-well guard-ring is also preferred due to the higher observed efficiency after integration. The implemented distributed-gain TIA (TIA1) and the impact of its on-chip integration with APDs have been also addressed more in detail in Appendix 3.

CHAPTER 5 GEIGER-MODE SIAPD AND PHOTON-COUNTER CIRCUIT INTEGRATION

5.1 Introduction

An APD can be applied in two different modes of operations: Proportional (linear or amplification) mode and Geiger (digital or trigger) mode. In Geiger-mode, the SiAPDs work as trigger devices rather than amplifying devices. Geiger-mode or Single-Photon Avalanche Diode (GM-APD or SPAD) is a modified PN junction, which allows single-photon detection. An infinite self-sustaining avalanche current flows through SPAD with impact of a single photon into its surface (active-area) which can be counted as a pulse at the SPAD output. This avalanche current has to be immediately suppressed (quenched) so that the duration of the avalanche current be as short as possible to avoid excessive power-dissipation and device destruction. This is generally accomplished via a Quenching circuit. Moreover, in order to count the number of consequently incident photons and minimize the dead-time, an external circuit called Reset-circuit is required in order to reset the SPAD bias to its initial condition after a hold-off time to prepare it for subsequent avalanche and counting the next photons. The resistance and capacitance of the SiAPD, quenching-circuit, silicon substrate, and resistive-load, all affect on the efficiency and response-time of the GM-SiAPD.

Single-photon detectors support a broad range of applications (Figure 5.1) such as low-intensity light detection and ranging (LIDAR), telecommunication systems, quantum cryptography and quantum information processing, molecular imaging and biomedical/brain imaging using computed tomography (CT-Scan), time-correlated single-photon counting (TCSPC) and near infra-red spectroscopy (NIRS). Single-photon avalanche photodiodes (SPAD) operating at Geiger-mode, has shown the potential for high-sensitivity and low-intensity light detection applications due to their internal gain characteristics. However the commercially available Quench-Reset circuits suffer from high-power consumption, large-size, relatively low-speed and high-noise which impede developing a portable, miniaturized and low-power photon-counting system for real-time brain imaging applications. High power-dissipation can drift the breakdown voltage, and change the SPAD response regarding to the detection efficiency and noise.

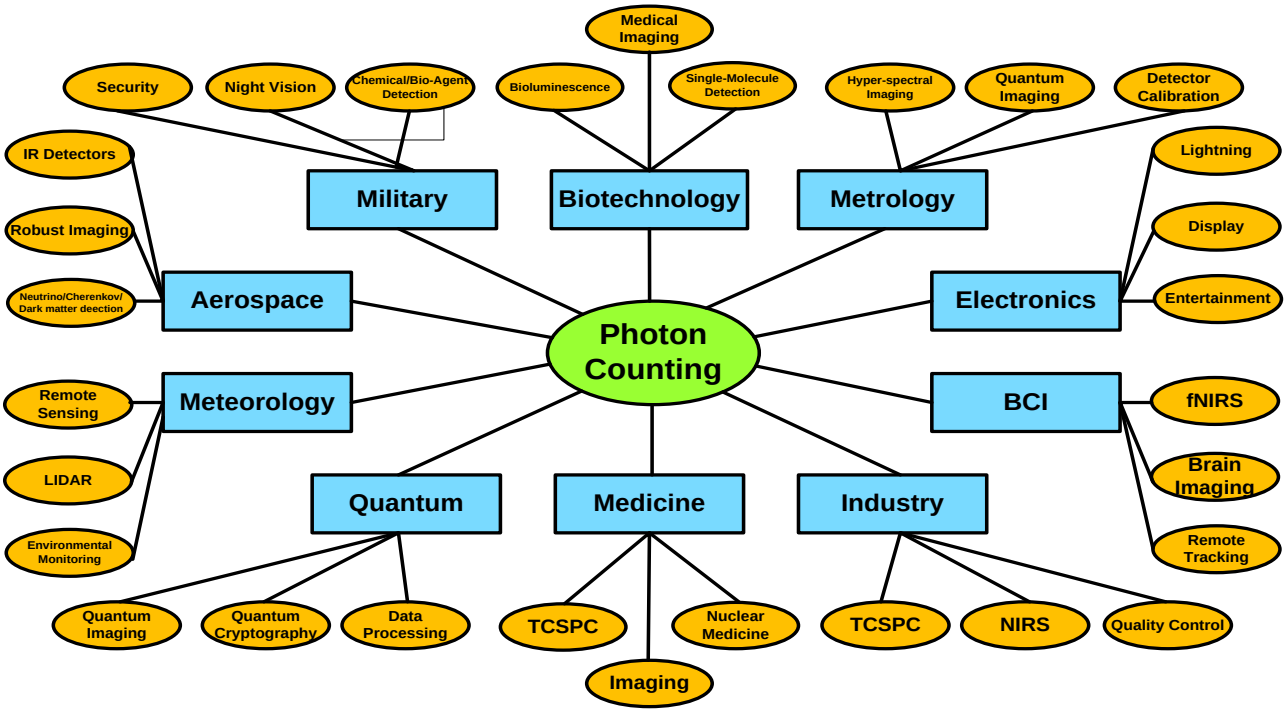


Figure 5-1: Photon-Counting applications

Delayed release of trapped charges due to the large charge-trapping in SPAD can retrigger the detector and cause false ignitions (after-pulsing). After-pulsing cause a non-linear distortion in photon-counting [178]. Decreasing the avalanche time duration will reduce the power-dissipation, charge-trapping and the optical cross-talk due to the minimization of the hot-carrier photon-emission [178],[249]. Here we have designed and implemented a miniaturized photon-counting system includes a high-speed and low-power photon-counter circuit integrated with silicon CMOS avalanche photodiode (SiAPD). This circuit accompanied with the CW-fNIRS channel, form a multi-modal brain imaging system using fNIRS (Figure 5.2). The main photon-counter circuit design methodology and its characteristics are explained in follow.

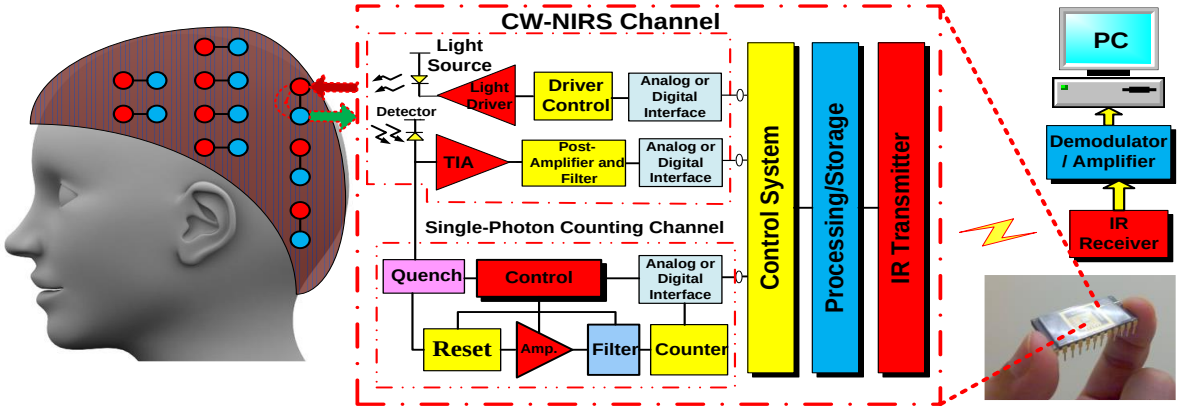


Figure 5-2: Block diagram of the proposed NIRS brain imaging system

5.2 Single-Photon Counter: Geiger-Mode SiAPD Implementation

The main available quench-reset techniques include: passive (PQ) [250], [251], active (AQ) [252], and mixed quenching (MQ) [126]. Here we have designed, implemented and examined all of these configurations and a new miniaturized photon-counting system includes a high-speed and low-power photon-counting circuit integrated with a GM-APD is implemented. This system is integrated in a multi-modal NIRS brain imaging system as shown in Figure 5.2 for real-time wireless detection of stroke and epilepsy seizures.

5.2.1 Implemented passive-quench circuits

The schematic of the implemented passive quench circuits (PQCs) are shown in Figure 5.3 (a)-(b) in two possible current and voltage mode configurations. The voltage-mode provides longer pulses, which might be convenient to visualize them in the oscilloscope but might hinder high-speed detection and the detector timing performance is not fully exploited. On the other hand, the current-mode output configuration allows high detection-rates [253], [126]. Here R_L is the load resistor (typically between 50kΩ-500kΩ) and RS provides matched termination for a coaxial cable (~50Ω). When no current flows in the circuit, the single-photon avalanche diode (SPAD) is reversed biased at V_{dd}. When a photon arrives a photo-generated current flows through the APD. The photo-current flows through R_L at this time and it causes the voltage in APD cathode and therefore its bias voltage reduce and suppresses the avalanche current. The large RC time-constant of PQ circuit (R_{in}×C) prevents the bias voltage from dropping rapidly.

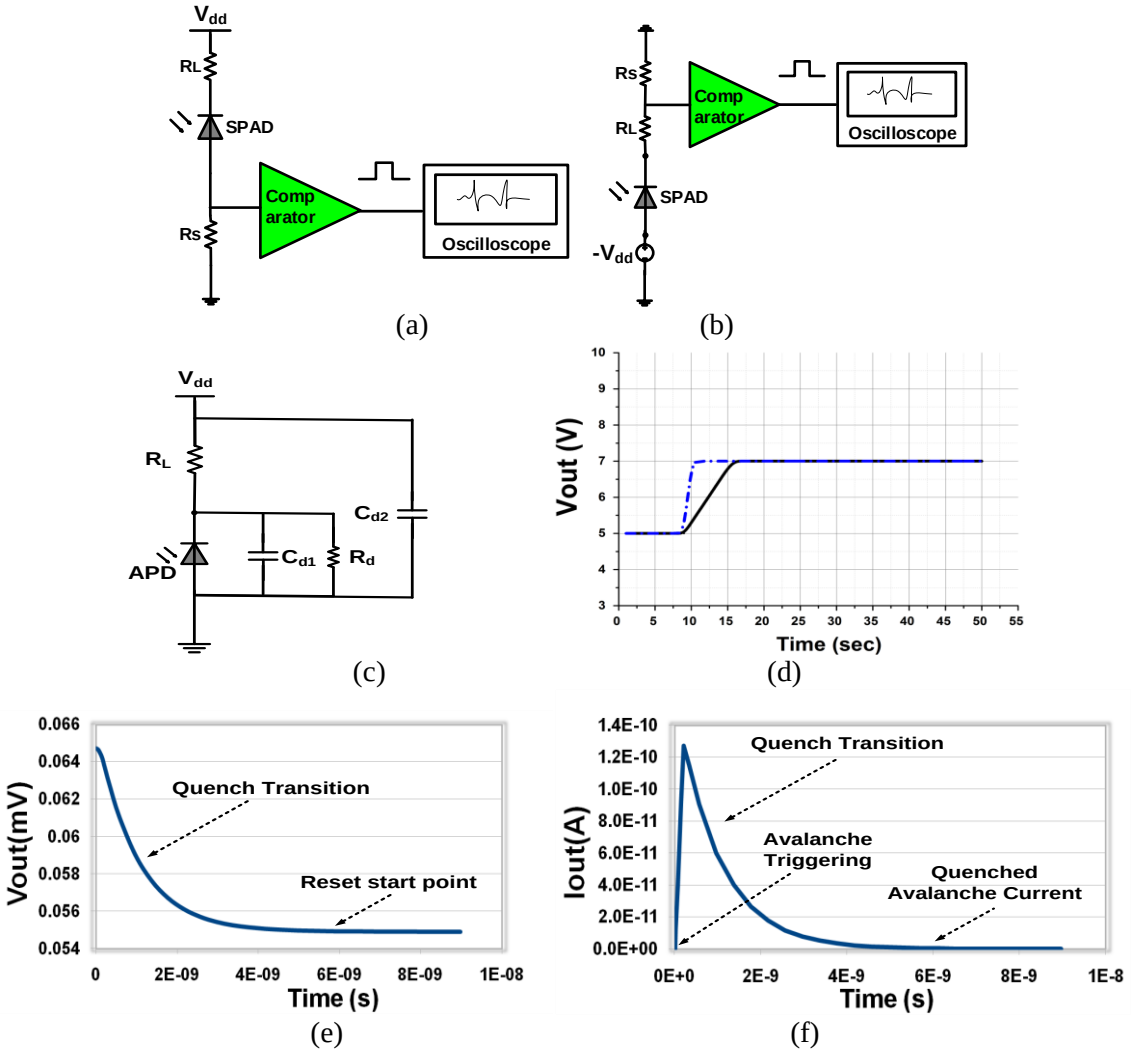


Figure 5-3: Schematic of the passive quench circuit in two possible current-mode (a) and voltage-mode (b) configurations. The PQ equivalent circuit (c) and its simulated output signal (d). The output signal (d)-(g) with C_{d1} = 3 pF, C_{d2}= 5 pF, V_{BR} = 9 V, V_{dd} = 3 V, R_L= 200 kΩ, and R_d = 1 MΩ. The APD cathode voltage (g) and current (h) in response to single-photon arrival.

This results in an avalanche quenching delay and hence inaccuracy in the photon-arrival detection and increases the power-consumption which introduce a higher temperature in SPAD. However the PQC is the simples quenching technique, but it suffers from low-speed and high power-dissipation and it is usually bulky due to its high-value resistor (R_L). It also limits the maximum operating frequency (< few hundred kHz) with large-area devices, making it impractical in most applications. Figure 5.3 (c) shows the equivalent circuit of PQ. Here the R_L represents the load resistor that recharges the APD after it has fired and turned off, C_{d1} represents the capacitance

associated with the cable from the APD to the oscilloscope, and C_{d2} represents the capacitance associated with the cable from the constant voltage supply V_{dd} to the load-resistor (R_L). R_d is the input impedance associated with the oscilloscope, i_L is the current through the load-resistor at any time, and V_d is the diode voltage sampled by the oscilloscope [71].

In Fig. 5.3 (e) and (f) the APD cathode voltage and current in response to single-photon arrival are plotted. They can also be used with large-area devices where high counting rates are not a requirement. Since we require large-area APDs for our application that is expected to count photons at high-speed ($\geq$ 1MHz), PQ is not a feasible option. PQ is suitable for APDs having small area and small RC time contacts since it can be operated at higher speed. They can also be used with large area devices where high counting rates are not a requirement.

5.2.2 Implemented active and mixed quench circuits

In order to achieve faster quenching, active-quenching circuit (AQC) is used. This method forces back on the APD to drop the bias-voltage much quicker enabling significant speed improvements over the PQ method. This technique offers high-accuracy, lower after-pulsing and lower power-consumption (hence less heating of the SPAD). Dead-time of the circuit does not depend on the component values and can be accurately controlled, hence determination of precise dead-time is possible for satisfactory circuit operation. However, these advantages achieves with the expense of stringent circuit requirements. It is difficult to design an effective AQ circuit and it needs extra and complicated ultra-precise circuitry to reduce propagation delays as well as stray capacitances.

We have implemented a quench-reset circuit in [254],[255] which is a combination of the previously applied active and passive techniques to be used along with the APD in Geiger-mode. It is applied a hybrid approach, known as mixed-quenching circuit (MQC) [256]. Here, passive-quenching is used as the first stage to limit the avalanche-current to a low-value, followed by the application of a quench-pulse during the quench delay-time and a reset-pulse to recharge the SPAD back to the reverse bias-voltage higher than V_{BR}. This method adopts a simpler design while still allowing some control over the dead-time and the use of a voltage-pulse to speed-up the quenching. The value of the load-resistor that provides the initial passive-quenching action

can be lower as compared to pure PQ since the actual quenching is done by AQC block [256]. However, the switching delays related to the relatively large parasitic capacitances and high-value PQ resistance of the circuit limit the performance and the quenching-speed of the MQC [257],[249],[258] and it needs more extra complicated circuitry and extra size [111],[259],[260],[261].

The schematic of the another proposed and implemented mixed Quench-Reset circuit is shown in Figure 5.4 [117]. As shown in this Figure, the circuit includes a Quench-block, a Reset-block, and a Control-block. In this circuit, the transistor M1 is biased in common-source mode with M3 as an active nMOS load. The transistor M4 is used as diode to provide the self-adjusting bias to the load M3 (the same for M2 and M6 which provide the self-adjusting bias to M_{Reset} and M5 respectively). Here the M_{Quench} and M_{Reset} are the main transistors for Quenching and Resetting the APD. The transistor M_{Select} is ON by default but it can be used to torn ON/OFF the Quench/Reset process or in APD arrays to select a specific row of photodetectors. This transistor (M_{Select}) connects the transistor M_{Reset} to APD cathode and charging the APD to the V_{BR}. By incident of the photon, the avalanche is initiated. This cause an voltage drop across APD. The M1 transistor amplifies the signal with a phase-shift. The amplified output of the M1, turns on the M_{Quench} transistor which pulls down the APD bias voltage bellow the V_{BR}. This quenches the APD output and the avalanche process would be completed. The Quench and Hold-off times can be controlled using Control-block connected to the M_{Select}. If the M_{Select} be activated by control block after a controllable hold-off time, then the M_{Reset} transistor, resets the APD by biasing it over its breakdown voltage. The generated pulse from the digitizer is detected by the D-flip flop, which is rising-edge sensitive. The APD cathode voltage is maintained constant during the hold-off period and then an enable pulse is generated. It discharges the APD back to its genuine operation level by activating low-resistance M_{Select} for detecting the next photon. The hold-off time is chosen with respect to the $R_{hold} \times C_{hold}$ value. The enable pulse for activating M_{Select} is generated through a NAND gate, followed by an inverter. The reset process should be as fast as possible to avoid dark-current noise. The reset-time for the designed circuit is 1-4ns. The choice of hold-off time is an application-dependent issue. In fact, there is a unique choice for the given application which might be affected by the nature, density and lifetime of the generated traps in

specific APD. The hold-off time should be long enough to allow trapped carriers to be emitted and minimizes the after-pulsing and on the other hand, short enough to avoid limiting the repetition rate which may intervene the system settling time fetching new photon detection procedure [117], [262], [263]. The measurement results are shown in Figure 5.4(d) and the main characteristics of the circuit are summarized in Table 5.1.

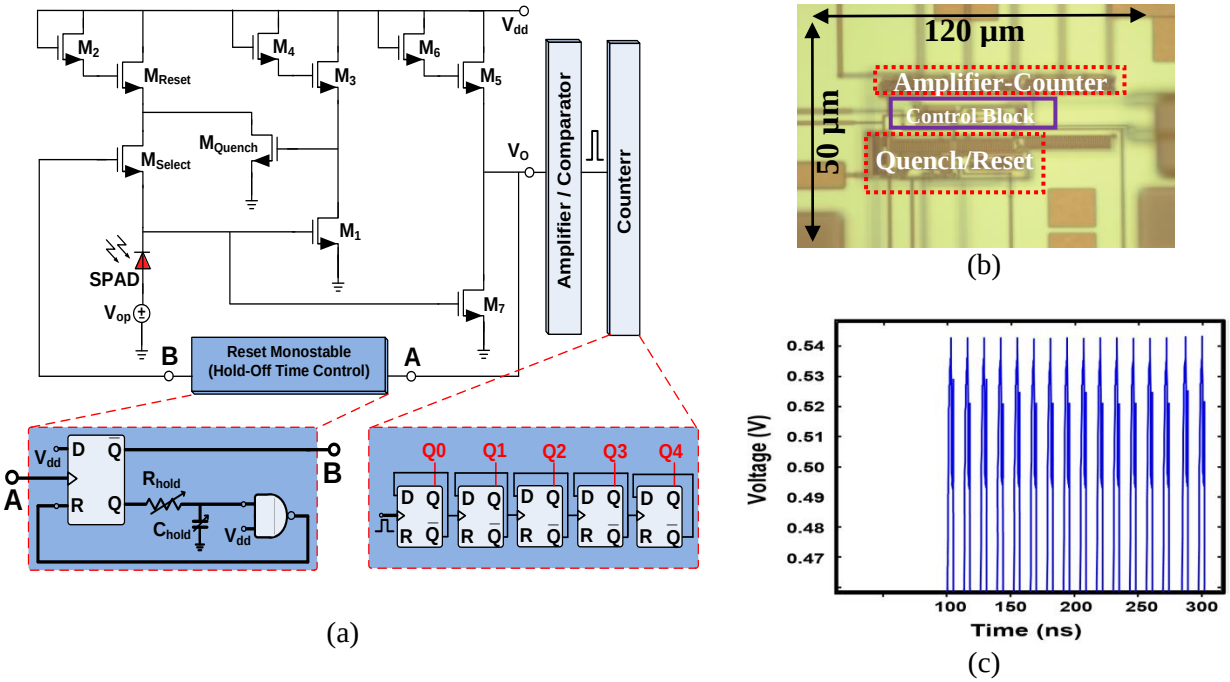


Figure 5-4: Schematic of the implemented Active-Mixed Quenching circuit (a). The microphotograph of the fabricated IC using TSMC CMOS 180nm technology (b), and the circuit response to multiple-photons arrival (d).

Table 5.1: General Characteristics of the implemented Mixed Quench Circuit using TSMC CMOS 180nm technology

Parameter	Simulation	Measurement
CMOS Technology	0.18 µm	0.18 µm
Power-consumption	2.14mW	1.70mW
Input Impedance	2 Ω	2.8 Ω
Output Impedance	1.58 kΩ	1.24 kΩ
Quench Time	3ns	100-200 ns
Dead-Time	7ns	7 ns

5.2.3 The new controllable mixed quench technique

Here we have developed a new controllable mixed-quench (CMQ) technique using CMQ circuit (CMQC) shown in Fig. 5.5, by modifying the mixed quench technique originally introduced in [256] suffering from high power-consumption, low dynamic-range and complexity. Here a timing-circuit controls the dead-time (quench+reset time). The dead-time of the circuit does not depend on the component values and can be accurately controlled to be matched with desired circuit operation. Using implemented CMQC, reduced the required size of load-resistor (R_L) and so the power-consumption, charge-trapping, after-pulsing and the optical cross-talk and also improved the performance by quicker detection of the photon in a wider dynamic-range optical input. In quiescence condition, the cathode of SPAD is biased to V_{dd} (usually 5-10% above the breakdown voltage for achieving higher sensitivity) through R1 and is ready to detect a photon. The onset of the avalanche current starts a passive-quenching action and the voltage drop across R1 reduces the voltage at the SPAD cathode. As such, S_{sense} goes in deeper conduction and the voltage drop caused by R3, turns the quench transistors ($S_{quench1}$ and $S_{quench2}$) ON via $S_{feedback}$. This starts the active-quenching action by quickly pulling the SPADs cathode down to ground. This brings the reverse bias of the SPAD below breakdown and the avalanche current quickly dissipates. The quench transistors ($S_{quench1}$ and $S_{quench2}$) are then turned OFF and the three parallel reset transistors (S_{reset1}, S_{reset2}, and S_{reset3}) are turned ON. The reset transistors are activated by an output pulse from the reset monostable which triggers with the end of the hold-off period. These reset transistors are equivalent of the three low-resistance transistors, which reset the quiescent bias of the SPAD and bring the SPAD cathode voltage back to detect the next photon. Short duration of the reset-time decreases the dead-time between photon-counts [264], [265]. It has to be note that in this circuit the excess voltage V_E, is given by:

$$V_E = V_{dd} + \left|V_{op}\right| - V_{BR} \tag{5.1}$$

where the bias-voltage is provided by circuit supply-voltage (V_{dd}) and a DC voltage (V_{op}) connected to the APD anode. The SPAD performance is directly proportional to the amount of the excess electric bias-voltage above the breakdown-voltage. So this MQC circuit improves the performance comparing to the PQC, due to the significant influence of the V_E on detector

performance. Using this circuit, offered a faster quenching with lower power-loss and hence less-heating of the SPAD. In this system, the APD is biased just below the breakdown-voltage and a gated-pulse is used to drive it above breakdown for a short duration. An incoming photon during this gated-pulse triggers the avalanche leading to a large current (Figure 5.5(b)) [183].

Due to the complementary action of the active quench circuit (AQC) in MQC in order to suppress more the initially quenched avalanche by the passive-quench circuit (PQC), there is more flexibility in choosing the PQ load (RL) [199]. Therefore by reducing the load-resistor (R_L) one can achieve a quicker photodetection. By increasing the light-intensity received by the APD, the current-flow through the APD and the series-connected resistor (R_L) also increases. The resulting increase voltage-drop across the R_L, decreases the bias-voltage across the APD, so that the gain of the APD is reduced. Therefore the dynamic-range of the optical input of the APD will be increased for a fixed dynamic-range of electrical output-voltage. In this circuit a current-mode PQ circuit is applied at the first stage which increased the detection-rate comparing to the voltage-mode PQ circuit with longer pulses. The incident light intensity information is obtained by counting the pulses during a certain time-frame or by measuring the average time-interval between successive pulses. In order to implement the CMOS SiAPDs characterization protocol, we have developed several experimental setups explained in chapter 3. The test setup secures the wafer to the probe station platform via vacuum and uses small probes to contact the metal pads for specific devices. A dark covering was used to block any stray light, which would affect the measurements, and all light sources in the room were turned off. The background light leakage was measured using a calibrated large-area photodiode [71]. In order to reduce the excess-noise and be able to detect high-rate array of photons, the dead-time is minimized. The measurement set-up for circuit characterization is shown in Figure 5.5(c). The SPAD Response-speed (rise-time) can be defined using cutoff frequency determined by the RC time-constant as: $t_r = 0.35/f_{c,RC}$ where $f_{c,RC} = 1/2\pi C_t R_L$. The rise-time of the output signal is a few fs. The decay-time depends on the recovery-time thus on the quenching circuit, which for the PQ the time-constant is given by the RC product (< 50ns). Both the rise-time and decay-time increase with the total capacitance of the APD. The APD capacitance increases with its area with typical values being 1 pF for a 1 mm² APD and 30 pF for 400mm² APD. Figures 5.5 (d)-(f) show the outputs of the implemented CMQC circuit in response to the single and multiple photon arrivals.

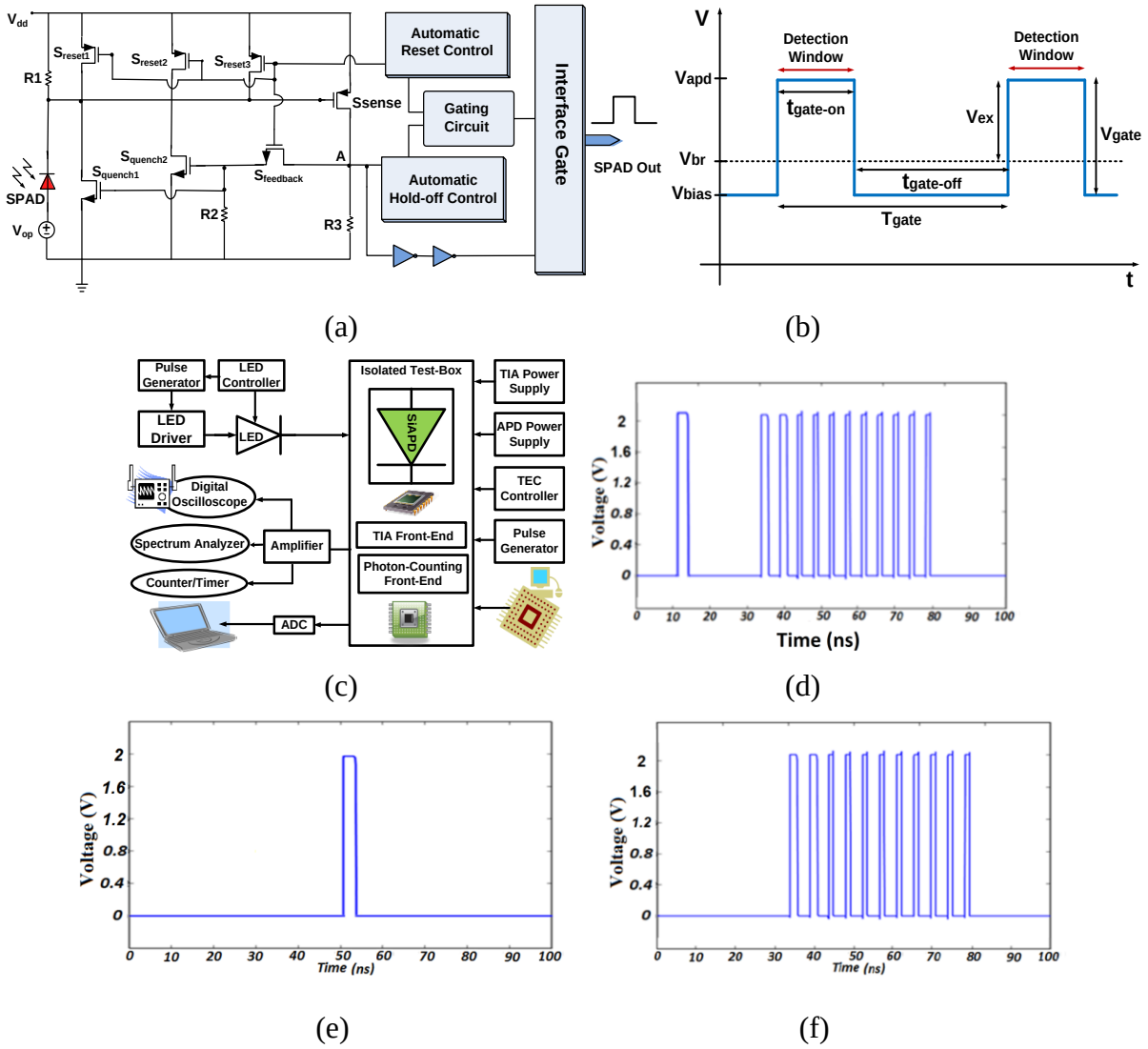
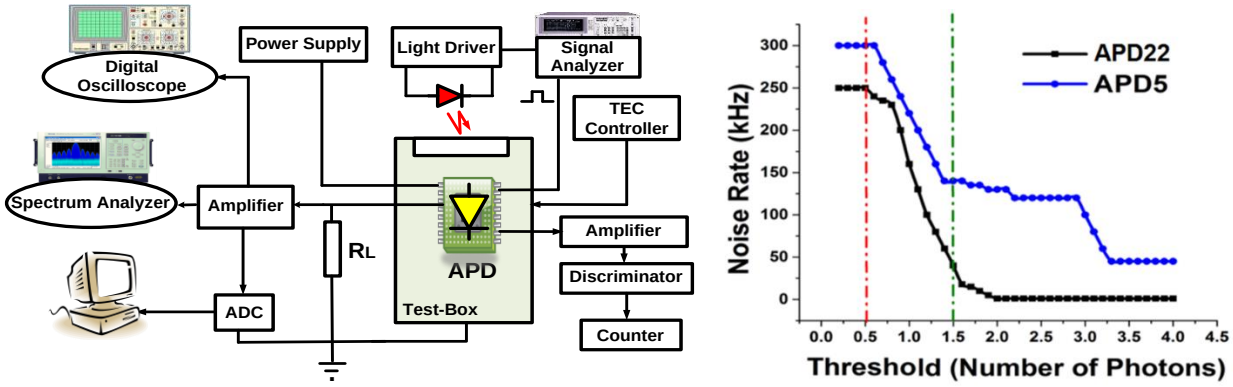


Figure 5-5: Schematic diagram of the implemented controlled mixed quenching circuit (a) and the applied Gated SPAD biasing technique (b). The applied measurement set-up (c) and the output response (d). The APD cathode voltage in response to single-photon arrival (e) and multiple-photon arrivals between 35ns-80ns (f).

The electronic setup for Dark-Count Rate (DCR) measurement is shown in Figure 5.6(a). Here the SiAPD is placed into a thermally stabilized light-tight box and the number of noise pulses generated per unit time is measured as a function of the discriminator threshold as established in [185]. The results for APD5 and APD22 are shown in Figure 5.6(b).

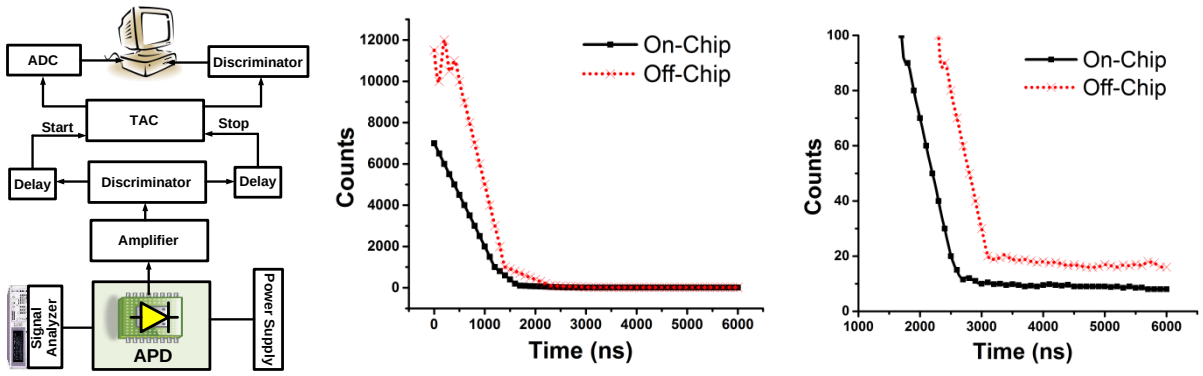


(a) (b)

Figure 5-6: Experimental setup for DCR measurement (a), and the measured noise rate vs threshold for APD5 and APD22 (b).

Here the threshold is normalized to the one-photon signal amplitude. High-power dissipation can drift the breakdown voltage, and change the SPAD response regarding to the detection-efficiency and noise. Delayed release of trapped-charges due to the large charge-trapping in SPAD can also retrigger the detector and cause false ignitions (after-pulsing). After-pulsing causes a non-linear distortion in photon-counting. Decreasing the avalanche-time duration has reduced the power-dissipation, charge-trapping and the optical cross-talk due to the minimization of the hot-carrier photon-emission.

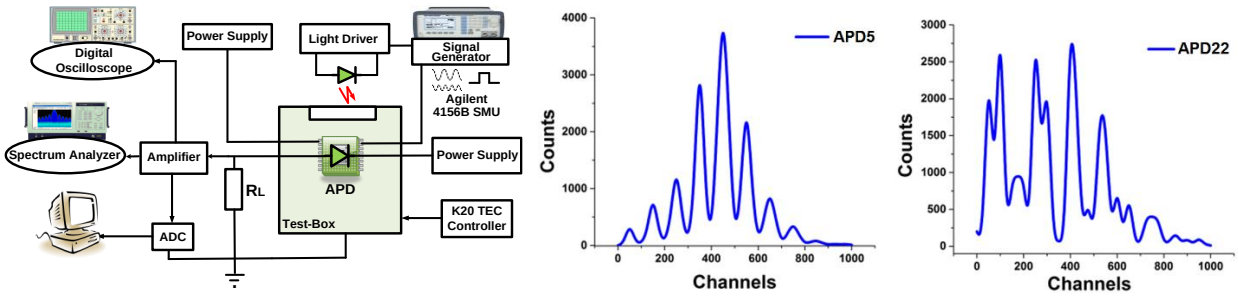
The electronic setup for after-pulse noise measurement is shown in Figure 5.7 (a) based on the applied technique in [266] and [185]. Here the start and stop inputs of the time-to-amplitude converter (TAC) are introduced by delayed-outputs of the discriminator. The discriminator introduces two fast logic outputs in response to the amplified output of the SPAD. The timing and delay has been precisely calibrated so that having a self-coincident peak below the overal TAC threshold and the system be trigerred only when there is a subsequent pulse (between 1ns and full-time range of 1ps) after the main detected signal. Then the distribution of the time intervals between 2 subsequent APD signals have been measured. The measured results for both on-chip and off-chip APDs are shown in Figs 5.7(b)-(c).



(a) (b) (c)

Figure 5-7: Experimental setup for afterpulse measurement (a), and the measured noise rate vs threshold for APD5 (b) and with zoom in steady-state (c).

The **Multiplication-gain** depends on the bias voltage. Uncertainties on the gain measurement directly affect the PDE values. By setting the light source intensity at various levels, the charge spectrum for each APD has been measured. The Gain measurement set-up is shown in Figure 5.8(a) based on the technique applied in [185]. Here in additional to the under test APD, a callibrated APD also has been used as a reference. The gain is measured by calculating the photo-current ratio between the under-test APD and the reference APD and also by computing the average spacing between two subsequent peaks in terms of charge-to-digital converter (QDC) Channel. Figures 5.8(b)-(c) show the measured gains of the proposed APD5 and APD22.



(a) (b) (c)

Figure 5-8: Experimental setup for the multiplication-gain measurement (a), and the measured gain for APD5 (b) and APD22 (c).

The **PDE** measurement setup is shown in Fig. 5.9(a). The PDE has been measured using two different techniques applied in [185] as follow:

(a) The Photo-current method consists in comparing the photocurrent of the characterized detectors with respect to that of a calibrated reference SPAD. In this case, the setup apparatus of Fig. 5.9(a) is simplified by substituting the amplifier, the discriminator and the counter with an ammeter. In practice we had two identical systems, one for the tested and one for the reference detector, and simply we have measured the photo-generated current in both sensors. The PDE then is calculated as:

$$PDE = \left(\frac{I_{on}-I_{off}}{I_{on1}-I_{off1}}\right) \times \frac{1}{M} \times PDE_1 \times \frac{A_1}{A} \quad (5.2)$$

where I_{on} (I_{on1}), I_{off} (I_{off1}) and A (A_1), are the photocurrent, dark-current, and active-area of the under test SPAD (and reference SPAD), respectively. The M and PDE_1 indicate the Gain and PDE of the reference SPAD.

(b) The Photon-counting method is based on measuring the SPAD count-rate (CR) due to the real photo-events and comparing it to the photocurrent measured by the ammeter converted into the number of electrons per second. The PDE then is defined as follow:

$$PDE = \left(\frac{CR_{on}-CR_{off}}{I_{on1}-I_{off1}}\right) \times \frac{1}{e} \times PDE_1 \times \frac{A_1}{A} \quad (5.3)$$

In order to obtain the accurate measurements in the "Photon-counting" technique, we have adjusted the photon-flux level in such a way that the reference detector was still sensitive and the detectors were safely in the single-photon regime with negligible pile-up (similar to the applied technique in [133]). Figure 5.9(b) shows the measured PDE for APD18 and APD20.

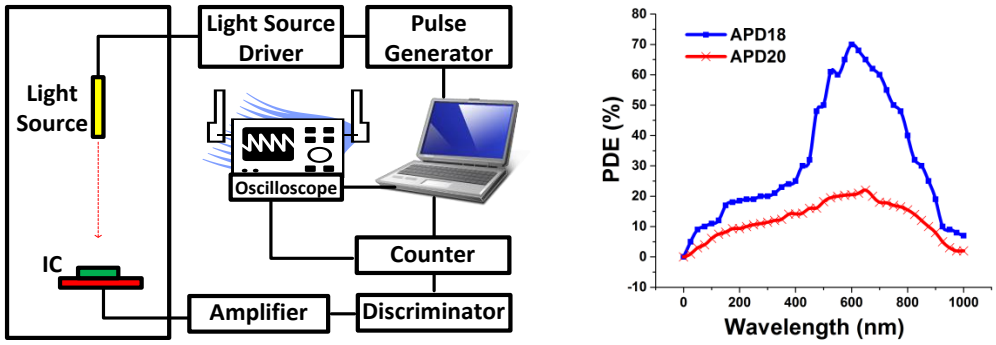
In the single-photon counting detector, the signal is determined by counting individual events of charge released by light absorption. The signal is then amplified (using TIA) and, if the signal exceeds an adjustable threshold, a photon-absorption event is digitally counted. Here the SiAPD is placed into a thermally stabilized light-tight box and the number of noise pulses generated per unit-time is measured as a function of the discriminator-threshold as established in [185]. Here the threshold is normalized to the one-photon signal amplitude.

It should be noted that, the single-photon detection experiments, don't necessarily generate a "single" photon. Generally a lots of photons are generated (for example using a 60 watt light bulb generates about 10^{20} photons per second) and then using filters to make sure that the photon-flux is exceedingly low, amounting to only one photon at a time over long periods of time (such as in

Young's double-slit experiment with only one photon at a time). More information can be found in [267] and [268]. Further work is required in order to realize a single-photon source and in order to prove that we have only a single-photon contributes in each output pulse [269]. The single-photon source can be realized using quantum-dots (QDs), the nanoscale semiconductor materials that can confine photons in 3 dimensions and release them after an empirically measurable decay-time (used to calculate the photon emission-rate from QD) depended on the applied material and with a known frequency (used to calculate the energy of a single-photon). If the peaks at the detector are further apart than the decay-time and each peak be measurable to a single-photon's energy, then we can conclude that we have a beam of a single-photon.

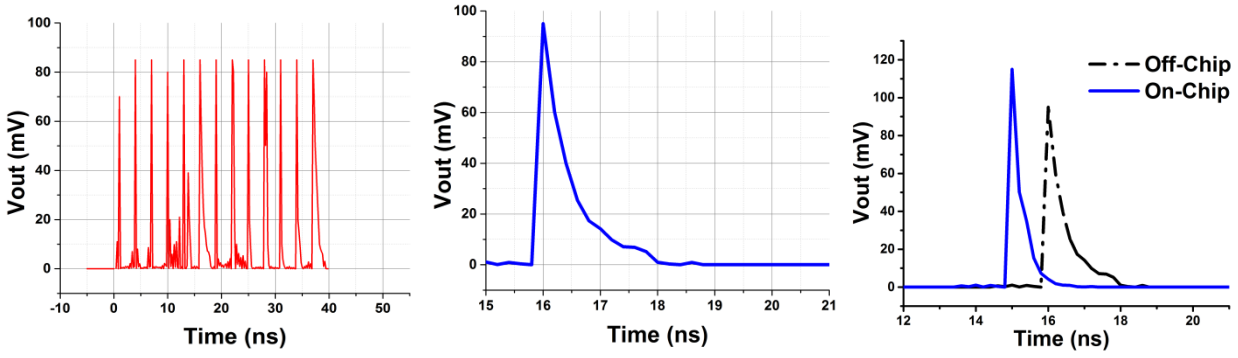
In order to prove that we have single-photons, we need to measure the time-interval between two consecutive photons and prove that no photons have zero time-intervals between them (this is called antibunching). The fluorescent antibunching can be measured using Hanbury-Brown and Twiss interferometer. It uses 2 APDs. A beam-splitter directs about half of the incident photons toward the first APD and half toward the second APD. One is used to provide a ‘start’ signal, and the other, which is on a delay, is used to provide a ‘stop’ signal. By measuring the time between ‘start’ and ‘stop’ signals, one can form a histogram of time delay between two photons and the coincidence count. The maximum counting-rate is limited by both the saturation of the detection electronics and the pile-up distortion effect, arising when more than one photon reach the detector during the same measurement time-slot. Here only the first photon can be detected due to the dead-time of the photodetector front-end (APD and the integrated electronic circuit), which prevents to acquire a late photon when an early photon has been detected at the same time. One applied solution was reducing the injected optical-power into the APD in order to reduce the number of detectable photons, and increasing the measurement-time. The light-source amplitude has been gradually decreased in a double slit experiment, and the transition from continuous bright and dark fringe has been observed on the screen to a single-dot at a time which has been considered for single-photon detection experiments. A stack of several metallic variable circular attenuators is used right before the injecting fiber in order to keep the total count rate within single-photon counting statistics to avoid pile-up distortion [269].

The Scope capture of single-photon events are shown in Figures 5.10 (a)-(b). The comparison of off-chip and on-chip integrated photon-counter responses as shown in Figure 5.10(c) shows higher SNR in additional to a faster response (2-5 ns). The main characteristics of the proposed techniques are summarized in Table 5.2 based on the simulation and measurement results. The results show that using this circuit, faster quenching resulted in lower-power loss and hence less-heating of the SPAD. Comparing the on-chip integrated and the individual off-chip APD results show that the on-chip integration of the APD and photon-counting circuitry has reduced the after-pulsing and increased the sensitivity accompanied with a lower power-consumption.



(a) (b)

Figure 5-9: (a) Schematic view of the PDE measurement setup. (b) The PDE characteristics of the APD18 and APD20.



(a) (b) (c)

Figure 5-10: The Scope capture of single-photon events (a), and close-up view of a single event (b). Comparison of off-chip and on-chip integrated photon-counter responses (c).

Table 5.2: Characteristics of the proposed system

Reference		CMOS Tech.	Supply Voltage	Power (mW)	Quench time	Dead time(ns)	Size	Control
[270]		-	High-Voltage	20	-	50	2mm×1mm	No
[271]		-	High-Voltage	20	-	20	1.1mm×1.2mm	No
[272]		-	High-Voltage	20	-	1	9740.6 μm^2	No
[273]		-	High-Voltage	-	-	40	50µm×100µm	Yes
[167]		**0.8µm**	**8V**	**20**	**21 µs**	**50ns**	**2mm²**	**No**
[221]		**0.8 µm**	**8V**	**20**	**8.7 µs**	**20ns**	**1.3mm²**	**No**
MQ [117]	**Sim**	**0.18µm**	**1.8**	2.14	**3ns**	7	50µm×120µm	Yes
	Mes*	**0.18µm**	**1.8**	1.70	**200 ns**	7	50µm×120µm	Yes
MQ([117])+APD*		**0.18µm**	**1.8**	**0.4**	**160 ns**	**7**	50µm×120µm	Yes
PQ*		**0.35µm**	**3V**	**1.3**	**250µs**	**90ns**	**2mm²**	**No**
AQ*		**0.35µm**	**3V**	**0.9**	**200ns**	**60ns**	**1.1mm²**	**No**
MQ*		**0.35µm**	**3**	**0.2**	**30ns**	**10ns**	**1.5mm²**	**Yes**
CMQ*		**0.18µm**	1.8	**0.4**	**10ns**	**2ns**	**0.1mm²**	**Yes**
CMQ+APD*		**0.18µm**	1.8	**0.1**	**8ns**	**2ns**	**0.1mm²**	Yes

*The results measurements are based on bare-die wafer.

5.3 Conclusion

In order to operate the SiAPD in Geiger-mode for single-photon counting, a new controllable photon-counting system was introduced and implemented in this chapter using standard CMOS technology. It includes a hold-off time control and an on-chip counter integrated in a small-area with a fast quench-rest, low power-consumption and low-noise characteristics. It exhibits a fast quench-time with a low power-consumption and less-complexity accompanied with more flexibility and dynamic-range of operation by developing an adaptive and fast hold-off time control on the available traditional quench circuits. Decreasing the avalanche-time duration reduced the power-dissipation, charge-trapping and the optical cross-talk noise. Characterizing the implemented system in response to single and multiple photon detections show its preference specially regarding to the power-consumption, speed, controllability and scale. Integrating the SiAPD and photon-counting circuitry in additional to offering a higher fill-factor value, has reduced the after-pulsing and increased the sensitivity accompanied with a lower power-consumption. The controllable hold-off time implemented in this circuit reduces the after-pulses and makes the system adaptable with different applications. It exhibits a controllable hold-off (in the range of 1ns to 2µs) and reset-time (with minimum value of 6ns) and a short quench-time of 3ns. The implemented MQC and CMQC techniques and the impact of on-chip integration of APDs with quench circuit, have been addressed in Appendix 4.

CHAPTER 6 GENERAL CONCLUSION AND RECOMMENDATIONS

6.1 Conclusion

The main building blocks of an fNIRS phototransceiver including APD, TIA, and photon-counter are designed and implemented in this thesis.

Several new SiAPDs have been implemented using standard 0.35µm and 0.18µm CMOS technologies in p+/n-well, p+/p-well, p+/p-sub, n+/p-well, n+/n-well, and n+/p-sub structures with guard-rings realized in different novel shapes and configurations. Impact of device simulation and its role in SiAPD fabrication are addressed based on our design, simulation and fabrication experiences. The effects of premature edge-breakdown (PEB) and available PEB-prevention (PEBP) techniques in silicon avalanche photodiode fabrication using the standard CMOS process have been scrutinized. The most common PEBP techniques are implemented following by a systematic study aimed at miniaturization, while optimizing the overall performance. By implementing different SiAPD structures, we have studied the geometric trade-offs involved in the design of deep-submicron SiAPDs. We studied the wavelength-dependency of the different SiAPDs and the optimal scales for NIR-sensitive APD design are selected. Inefficiency of the applied PEBP techniques and corresponding device simulations can lead to a low-performance or dysfunctional SiAPD and also significant discrepancy between simulation and measurement characteristics. In addition to the doping-profile and electric-field distribution in a SiAPD structure, the punch-through, high-tunneling and PEB effects should be considered to design a high-quality SiAPD using the standard CMOS process. The sharpness of the transition between band-to-band tunneling and the avalanche has to be considered as a critical design criterion. The p-well-, p-sub- and n-well-based PEBP techniques are evaluated and compared based on the simulation and fabrication results using standard CMOS process. The results demonstrate that the n-well guard-ring offers the most efficient PEBP technique. The p-well and p-substrate structures suffer from punch-through, high-tunneling and PEB. However, the SiAPD with the n-well-based guard-ring structure offers the highest sensitivity and PDP-to-DCR ratio characteristics and could be biased properly in the Geiger-mode. This technique offers a high-gain (~100), low-noise dark current rate (DCR = 40 Hz), high detection-efficiency (70%) APD with a low breakdown-voltage and high functionality-probability. A new PEBP technique has

been introduced based on the APD-Shaping. Using this technique (called Shaping-PEBP), implementing the APDs in Rectangular, Octagonal, Hybrid-Octagonal, Netted (Reticulated), Nested (Maze-Shape), Quadratic, and Hexadecagonal-shapes, have improved the APDs characteristics with a more efficient PEB-prevention. Using shaping-PEBP (SPEBP) technique has increased the functionality and offered ADPs with higher-PDE and less-noise compared to the conventional PEPB techniques.

Three new Transimpedance amplifiers have been introduced and implemented using standard CMOS technology with high gain-bandwidth product (GBW) and low-noise to be applied in a continuous-wave (CW) fNIRS. The first introduced TIA has been designed using distributed-gain concept combined with resistive-feedback and common-gate topology and offers high-transimpedance gain (up to 250 MV/A), tunable BW (1 kHz–1 GHz), extremely low input and output noises (100 fA/√Hz, 1.8 μV/√Hz), low power-consumption (0.8 mW), high-stability (phase-margin ≥ 40°), and robustness against power-supply variation (1–3 V). The implemented TIA also shows efficient results in two different bias voltages. The second TIA is a distributed-gain 4-stage amplifier, targeted towards offering high-GBW. This TIA offers a low power-consumption (4mW), high transimpedance-gain (up to 250MV/A), tunable wide-BW range (100kHz - 1MHz) and very low-input and output noise (280fA/√Hz and 1.5mV/√Hz). A new Logarithmic TIA (LogTIA) with automatic gain control and ambient-light rejection is also introduced for low-intensity light detection applications. This TIA has been implemented in 2 different CMOS technologies. Using AGC and noise-rejection in LogTIA have reduced the input current noise (with factor of 0.1) and have increased the GBW (with factor of 6.8) compare to the regular LogTIA.

In order to operate the SiAPD in Geiger-mode for single-photon counting, a new high-speed, low-power and controllable photon-counting technique is introduced and implemented using standard CMOS technology. It includes a hold-off time control and an on-chip counter integrated in a small-area offers a fast quench-time (< 10ns) with a low-power consumption (0.6 mW) and less complexity accompanied with more flexibility and dynamic-range of operation by developing an adaptive and fast hold-off time control on the available traditional quench-circuits. Decreasing the avalanche-time duration has reduced the power-dissipation, charge-trapping and the optical crosstalk noise. Characterizing the implemented device in response to single and

multiple photon detections show its preference specially regarding to the power-consumption, speed, controllability and scale.

The main effects of on-chip integration on the performance and efficiency of the silicon avalanche photodiode (SiAPD) and photodetector front-end have been addressed in this thesis based on the simulation and fabrication experiments. The on-chip integrated SiAPDs show higher signal-to-noise ratio (SNR), sensitivity and detection-efficiency comparing to the separate SiAPDs. The integration does not show a significant effect on the gain and preserves the low power-consumption. Using APDs with p-well guard-ring is preferred due to the higher observed efficiency after integration. The on-chip integrated APDs with the TIA preserved the high-performance characteristics of the both APDs and TIA, while offered a more miniaturized photodetector front-end dedicated to low-intensity light detection applications. The integration improved the SNR, sensitivity, fill-factor (FF) and PFR with no significant change in power and gain values. Using APDs with larger active areas and applying p-well guard-ring is also preferred due to the higher observed efficiency after integration. We have also shown that on-chip integration of the APD and photon-counting circuitry, in additional to offering a higher fill-factor design, reduces the after-pulsing and increases the sensitivity accompanied with a significant decrease in power-consumption. The on-chip integration has increased the SNR in additional to offering a faster response (2-5 ns) compared to the non-integrated APD and photon-counter.

6.2 Future Work

Though this thesis covered the main design requirements and issues towards implementing an efficient NIRS photoreceiver front-end, but there is still room for improvement and future work:

(a) SiAPD

1. Supplementary testing scenarios would further distinguish the various sources of imperfection in SiAPDs implementation using standard CMOS process, leading to better overall characterization of the devices.
2. Aside from additional measurements, changes to the simulation methodology may also lead to more unique results. Possible improvements to the simulation parts of this thesis

include the addition of a multiphysics device simulation (using COMSOL or TCAD) as well as analytic study based on the theoretic models are recommended.

3. Though the testing described in this thesis is valuable, the measurement setups for SiAPD characterization both in Linear and Geiger mode are mainly affecting on the measured results. Study and evaluation of different possible SiAPD characterization set-ups and offering the best configuration for each application would be very valuable.

(b) TIAs

1. Using implemented logarithmic TIA (LogTIA) to develope a single-chip fNIR and for on-chip HbR/HbO characterization.
2. Implementing the introduced TIAs in a higher CMOS technology (65nm, 90nm, or 180nm), which may reduce the power-consumption and noise-level of the implemented circuits.

(c) Photon-Counter Circuit

1. The packaging and applied pad effected on APDs with a variable deviation on the measurements. It is highly recommended to investigate these effects in detail and to offer the most appropriate pad for layout design. Based on the experience of this work, using low-impedance, and simple pads without any ESD protection would be preferred.
2. More investigations on the single-photon measurement set-ups has to be done in order to insure counting a single photon and distinguish/discriminate the thermally generated photons.

(d) Integration

1. Another worthwhile improvement to this project would be the inclusion of a dedicated LED and its on-chip integration with a collection of the best already implemented SiAPDs, a TIA, a photon-counter and the control circuit. This would offer a single-channel fNIRS phototransceiver and allows a more detailed investigation on the integration impacts.

2. Developing a sensors-network of the proposed photodetector front-end, covering the head through a custom made cap is recommended as a future work.
3. The future work would be integration of this Photoreceiver front-end with electroencephalography (EEG) and wireless integrated circuits using standard CMOS process towards a wireless multimodal (fNIRS+EEG) imaging system for long-term, real-time and wireless brain monitoring application.

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APPENDIX 1 – LIST OF PUBLICATIONS

In follow, are the list of publications:

a) Peer Reviewed and Refereed Journal Papers

[1] **E. Kamrani**, F. Lesage, and M. Sawan, "On-Chip Integrated Photoreceiver for Real-Time Brain Imaging", Transactions of Japanese Society for Medical and Biological Engineering (Trans JSMBE), 2013.

[2] **E. Kamrani**, F. Lesage, and M. Sawan, "Low-Noise, High-Gain TIA Integrated with CMOS APD for Low-Intensity Light Detection in Near-Infrared Spectroscopy", IEEE Sensors Journal, vol. 14, no. 1, January 2014.

[3] **E. Kamrani,** F. Lesage, and M. Sawan, "Efficient Premature Edge Breakdown Prevention Technique for SiAPD Fabrication using Standard CMOS Process", IOP International Journal of *Semiconductor Science and Technology (JSST)*, 28(4), 045008, 2013.
(Top 20 most downloaded articles published in 2013, Free open access award)

[4] **E. Kamrani**, F. Lesage, and M. Sawan, "Fully On-Chip Integrated Photodetector Front-End Dedicated to Real-Time Portable Optical Brain Imaging", Optics and Photonics Journal (OPJ), Vol. 2. No. 4, pp. 300-313, December, 2012.

[5] **E. Kamrani**, A. N. Foroushani, M. Vaziripour, and M. Sawan, "Detecting the Stable, Observable and Controllable States of the Human Brain Dynamics", Open Journal of Medical Imaging (OJMI), vol. 2, no. 4, pp. 128-136, November 2012.
(The most popular paper in 2012-2013)

[6] **E. Kamrani**, "Real-Time Internet-Based Teleoperation", International Journal of Intelligent Control and Automation (ICA), Vol. 3, No. 4, pp. 356-375, November 2012. (Free submission and open access award)

[7] **E. Kamrani**, A. N. Foroushani, M. Vaziripour, and M. Sawan, "Efficient Hemodynamic States Stimulation using fNIRS Data with the Extended Kalman Filter and Bifurcation Analysis of Balloon Model", Journal of Biomedical Science and Engineering (JBiSE), vol. 5, no. 11, pp. 609-628, November, 2012.
(Free submission and open access award)

[8] **E. Kamrani,** and M. Sawan, "Wave Prediction and Delay Modeling for Teleoperation via Internet", Global Journal of Computer Science and Technology (GJCST), Volume 12 Issue 11 Version 1.0, pp. 41-47, June 2012.

[9] **E. Kamrani,** and M. Sawan, "Human Vision Inspired Technique Applied to Detect Suspicious Masses in Mammograms", Global Journal of Computer Science and Technology (GJCST), Volume XII, Issue X, Version I, pp. 33-35, June 2012.

[10] A. Sultana, **E. Kamrani**, and M. Sawan, "CMOS Silicon Avalanche Photodiodes for NIR Light Detection: A Survey", Journal of Analog Integrated Circuits and Signal Processing, Vol. 70, No. 1, pp. 1-13, 2012.

[11] **E. Kamrani**, "Extracting the prevailed patterns in recognizing the picture by the human vision", International Journal of Advanced Robotic Systems, Vol. 6, No. 3, ISSN 1729-8806, pp. 223-228, September 2009.

[12] **E. Kamrani**, F. Lesage, and M. Sawan, "A Portable Wireless NIRS System Combined with EEG for Bedside Monitoring of Stroke and Cardiac Patients", Submitted at IEEE Transactions on Biomedical Circuits and Systems (TBioCAS), 2014.

[13] **E. Kamrani**, F. Lesage, and M. Sawan, "High-Gain, Low-noise and High Efficiency SiAPDs", To be submitted at Journal of Optics Express, 2014.

[14] A. Chaddad, R. Chebli, **E. Kamrani** and M. Sawan, "Low Noise Front-End Receiver Dedicated to Hand-Held NIRS/EEG Acquisition System", To be submitted at Journal of Microelectronics, 2014.

b) Peer Reviewed and Refereed Conference Papers

[1] **E. Kamrani**, F. Lesage, and M. Sawan, "Towards an On-Chip Integrated Miniaturized System for Real-Time Brain Imaging", Proceedings of SPIE, Optics+Photonics, NanoScience+Engineering, San Diego, California, United States, 25 - 29 August 2013.

[2] **E. Kamrani**, F. Lesage, and M. Sawan, "Low-Power, High-Speed, Miniaturized and Controllable Single-Photon Counting Circuit Dedicated to Biomedical Imaging Applications", Proceedings of SPIE, Optics+Photonics, NanoScience+Engineering, San Diego, California, United States, 25 - 29 August 2013.

[3] **E. Kamrani**, F. Lesage, and M. Sawan, "Towards On-Chip Integration of Brain Imaging Photodetecors Using Standard CMOS Process", The 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'13), Osaka, Japan, 3-7 July 2013.

[4] A. Chaddad, **E. Kamrani**, J. L. Lan, and M. Sawan, "De-noising fNIRS Signals to Enhance Brain Imaging Diagnosis", 29th Southern Biomedical Engineering Conference (SBEC'13), pp. 33-34, Miami, FL, USA, May 3-5, 2013.

[5] **E. Kamrani**, A. N. Foroushani, M. Vaziripour, and M. Sawan, "Monitoring and Controlling of the Human Brain Dynamics", 29th Southern Biomedical Engineering Conference (SBEC'13), Miami, FL, USA, May 3-5, 2013.

[6] **E. Kamrani**, A. Chaddad, F. Lesage, and M. Sawan, "Integrated Transimpedance Amplifiers Dedicated to Low-Noise and Low-Power Biomedical Applications", 29th Southern Biomedical Engineering Conference (SBEC'13), pp. 5-6, Miami, FL, USA, May 3-5, 2013.

[7] **E. Kamrani**, F. Lesage, and M. Sawan, "On-Chip Single Photon Counting Electronic Circuitry Dedicated to Real-Time Brain Imaging Applications", 29th Southern Biomedical Engineering Conference (SBEC'13), pp. 61-62, Miami, FL, USA, May 3-5, 2013.

[8] **E. Kamrani**, M. Hamady, F. Lesage, and M. Sawan, "Modeling and Characterizing Optical CMOS Sensors for Biomedical Low-Intensity Light Detection", 29th Southern Biomedical Engineering Conference (SBEC'13), pp. 83-84, Miami, FL, USA, May 3-5, 2013.

[9] M. Ameri, **E. Kamrani**, S. Hashemi, and M. Sawan, "A Fast Quench-Reset Integrated Circuit for High-Speed Single Photon Detection", the 8th IEEE International symposium on Medical Measurements and Applications (MeMeA'13), pp. 179-182, Gatineau, Quebec, Canada, May 4-5, 2013.

[10] M. Hamady, **E. Kamrani**, and M. Sawan, "Modeling CMOS PIN Photodiode using COMSOL", Proceedings of the 24th IEEE International Conference on Microelectronics (ICM'12), Algeria, December, 2012.

[11] **E. Kamrani**, S. H. A. Yun, F. Lesage, and M. Sawan, "State-of-the-Art Logarithmic Transimpedance Amplifier With Automatic Gain Control and Ambient Light Rejection for fNIRS", Proc. of SPIE MIOMD-XI: 11th International Conference on Infrared Optoelectronics: Materials and Devices, Chicago, IL, USA, 4 - 8 September 2012, pp. 58-59.

[12] **E. Kamrani,** S. H. A. Yun, F. Lesage, and M. Sawan, "Optimal-Adaptive Control System for Low-Noise, Low-Power and Fast Photodetection in Functional Near Infra-Red Spectroscopy", Proc. of SPIE MIOMD-XI: 11th International Conference on Infrared Optoelectronics: Materials and Devices, Chicago, IL, USA, 4 - 8 September 2012, pp. 56-57.

[13] **E. Kamrani**, S. H. A. Yun, F. Lesage, and M. Sawan, "Near Infra-Red Light Detection Using Silicon Avalanche Photodiodes: Design Challenges in Standard CMOS Technology", Best Paper

Award, Proc. of SPIE MIOMD-XI: 11th International Conference on Infrared Optoelectronics: Materials and Devices, Chicago, IL, USA, 4 - 8 September 2012, pp. 54-55.

[14] **E. Kamrani**, F. Lesage, and M. Sawan, "Fast Photodetection in Functional Near Infra-Red Spectroscopy", Proc. of SPIE MIOMD-XI: 11th International Conference on Infrared Optoelectronics: Materials and Devices, Chicago, IL, USA, 4 - 8 September 2012, pp. 57-58.

[15] **E. Kamrani,** F. Lesage, and M. Sawan, "Premature Edge Breakdown Prevention Techniques in APD fabrication", The 10th IEEE International NEWCAS Conference (NEWCAS2012), Montreal, Canada, June 17-20, 2012, pp. 345-348 (Invited paper).

[16] **E. Kamrani**, F. Lesage, and M. Sawan, "Design and Implementation of an Integrated Functional Near Infra-Red Spectroscopy Photoreceiver for Real-Time Brain Monitoring", Best Paper Award, ReSMiQ symposium on Microsystems and networking: A necessary mix, A part of the ACFAS 80th conference, Montréal, May 7, 2012.

[17] **E. Kamrani**, and M. Sawan, "Fully Integrated CMOS Avalanche Photodiode and Distributed-Gain TIA for CW-fNIRS", The IEEE Biomedical Circuits and Systems Conference (BioCAS2011), San Diego, USA, Nov. 2011, pp. 317-320.

[18] **E. Kamrani**, A. Sultana, and M. Sawan, "Tunable, Low-Power, High-Gain Transimpedance Amplifier for fNIRS Photoreceiver Front-End", The 54th IEEE International Midwest Symposium on Circuits and Systems (MWSCAS), Seoul, Korea, August, 2011

[19] **E. Kamrani,** R. Chebli, A. Moradi, F. Lesage, and M. Sawan, "Fully Silicon CMOS On-Chip Integrated Low-Power Front-End for Simultaneous Wireless Monitoring of Neurovascular Brain Dynamics using Electroencephalography (EEG) and Near Infra-Red Spectroscopy (NIRS)", to be submitted at the IEEE International Conference, 2014.

c) Books and book chapters

[1] **E. Kamrani**, F. Lesage, and M. Sawan, "Photodetectors for medical imaging applications", in Photodetectors: materials, devices, applications, To be appeared in Woodhead Publishing CRC Press, London, 2014.

[2] **E. Kamrani**, F. Lesage, M. Sawan, “Near-Infrared Light Detection using CMOS Silicon Avalanche Photodiodes (SiAPDs),” in The Wonder of Nanotechnology: Quantum Optoelectronic Devices and Applications, M. Razeghi. L. Esaki, and K. von Klitzing, Eds., SPIE Press, Bellingham, WA, pp. 491-531, 2013.

[3] **E. Kamrani**, A. Ghaffari, and A. Saki, "Using Adaptive Fuzzy Control for tuning the Air-Fuel Ratio of Automobile Spark Ignition Engine", Advanced Technologies Book, InTech Press, ISBN 978-953-7619, 2009.

d) Workshops, Abstracts and Poster Presentations

Peer Reviewed and Refereed:

[1] **E. Kamrani**, F. Lesage, and M. Sawan, "A Fully On-Chip Integrated Photodetector Front-End for Real-Time Wireless Brain Imaging and Brain-Machine Interface Applications", The Annual CMC Microsystems Symposium, TEXPO 2013, Gatineau, Quebec, Canada, 15 -16 Oct. 2013.

[2] **E. Kamrani,** F. Lesage, and M. Sawan, "Optical EEG: A Novel Miniaturized Real-Time Non-Invasive Brain Imaging System Dedicated to Clinical Monitoring and Brain-Machine Interface Applications", The 2013 International Neurotechnology Consortium (INC'13) Workshop on NeuroDiagnostics, NeuroTherapeutics, Imaging and Grand Challenges, Osaka, Japan, July 03, 2013.

[3] **E. Kamrani**, F. Lesage, and M. Sawan, "Fully Integrated Phototransceiver dedicated to Brain-Machine Interface and Real-time Wireless Brain Imaging", The best paper award in 12th Research Day, Polytechnique Montreal, Montreal Canada, May 29-30, 2013.

[4] **E. Kamrani**, A. N. Foroushani, M. Vaziripour, F. Lesage, and M. Sawan, "Real-Time Monitoring and Modeling of Human Brain Dynamics", The best paper award in 12th Research and Innovation Day, Polytechnique Montreal, Montreal Canada, May 29-30, 2013.

[5] **E. Kamrani**, F. Lesage, and M. Sawan, "On-Chip Integrated Photoreceiver for Real-Time Brain Imaging", Late breaking research posters paper, The 35th Annual International Conference of the IEEE Engineering in Medicine and Biology Society (EMBC'13), Osaka, Japan, 3-7 July 2013.

[6] **E. Kamrani**, F. Lesage, and M. Sawan, "Design and Implementation of an Integrated Functional Near Infra-Red Spectroscopy Photoreceiver for Real-Time Brain Monitoring", The 2013 CIHR - Institute of Circulatory and Respiratory Health - Young Investigators (YI) Forum, Toronto, ON, Canada, May 27-29, 2013.

[7] **E. Kamrani**, F. Lesage, and M. Sawan, "Fully On-Chip Front-End Interface for Real-Time Optical Brain Imaging", ReSMiQ symposium on Microsystems and networking: Innovative Microsystems for the Future Health, A part of the ACFAS 81st conference, Université Laval, Quebec City, Canada, May 6, 2013.

[8] **E. Kamrani**, A. N. Foroushani, M. Vaziripour, and M. Sawan, "Monitoring and Controlling of the Human Brain Dynamics", 29th Southern Biomedical Engineering Conference (SBEC'13), Miami, FL, USA, May 3-5, 2013.

[9] **E. Kamrani**, A. Chaddad, F. Lesage, and M. Sawan, "Integrated Transimpedance Amplifiers Dedicated to Low-Noise and Low-Power Biomedical Applications", 29th Southern Biomedical Engineering Conference (SBEC'13), Miami, FL, USA, May 3-5, 2013.

[10] **E. Kamrani**, F. Lesage, and M. Sawan, "On-Chip Single Photon Counting Electronic Circuitry Dedicated to Real-Time Brain Imaging Applications", 29th Southern Biomedical Engineering Conference (SBEC'13), Miami, FL, USA, May 3-5, 2013.

[11] **E. Kamrani**, M. Hamady, F. Lesage, and M. Sawan, "Modeling and Characterizing Optical CMOS Sensors for Biomedical Low-Intensity Light Detection", 29th Southern Biomedical Engineering Conference (SBEC'13), Miami, FL, USA, May 3-5, 2013.

[12] A. Chaddad, **E. Kamrani**, J. L. Lan, and M. Sawan, "De-noising fNIRS Signals to Enhance Brain Imaging Diagnosis", 29th Southern Biomedical Engineering Conference (SBEC'13), Miami, FL, USA, May 3-5, 2013.

[13] **E. Kamrani**, S. H. A. Yun, F. Lesage, and M. Sawan, "Fully Integrated Near Infra-Red Photodetector for Real-time Wireless Brain Imaging", A Poster presented at SPIE MIOMD-XI: 11th International Conference on Infrared Optoelectronics-Materials and Devices, Chicago, IL, USA, 4 - 8 September 2012.

<u>Non-Refereed</u>:

[14] **E. Kamrani**, F. Lesage, and M. Sawan, "On-Chip Integrated Photoreceiver for Real-Time Brain Imaging", GRSTB (Groupe de recherche en sciences et technologies biomédicales) Symposium on Emerging Technologies in Imaging, Montreal, Canada, March 8th, 2013.

[15] **E. Kamrani**, F. Lesage, and M. Sawan, "Highly-Sensitive Near-Infrared Detectors Using Low-Voltage Silicon APDs", IOP LabTalk, Research highlights on Semiconductor Science and Technology, Published on March 20, 2013.

[16] **E. Kamrani**, F. Lesage, and M. Sawan, "Design and Implementation of an Integrated Functional Near Infra-Red Spectroscopy Photoreceiver for Real-Time Brain Monitoring", A paper presented as PhD Seminar in University of Montreal, Montreal, Canada, April, 2012.

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[4] **E. Kamrani,** F. Lesage, and M. Sawan, " Low-Noise, Low-Power, High-Gain SiAPDs for Ultra Low-Level Light Detection", Under submission, 2013.

[5] **E. Kamrani,** F. Lesage, and M. Sawan, "A Low-Noise, High Gain Logarithmic TIA", Under submission, 2013.

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APPENDIX 2 – PAPER #1

Efficient premature edge breakdown prevention in SiAPD fabrication using the standard CMOS process

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Efficient premature edge breakdown prevention in SiAPD fabrication using the standard CMOS process

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Abstract
The effects of premature edge breakdown (PEB) and available PEB prevention (PEBP) techniques in silicon avalanche photodiode fabrication using the standard complementary metal–oxide–semiconductor (CMOS) process are scrutinized in this paper. Impact of device simulation and its induced impacts on fabrication are addressed based on our design, simulation and fabrication experiences. Three most common PEBP techniques are implemented followed by a systematic study aimed at miniaturization, while optimizing the overall performance. The p-well-, p-sub- and n-well-based PEBP techniques are evaluated and compared based on simulation and fabrication results using the standard CMOS process. The results demonstrate that the n-well guard ring offers the most efficient PEBP technique. This technique offers a high-gain (~800), low-noise dark current rate (DCR = 40 Hz), high detection efficiency (70%) avalanche photodiode with a higher functionality probability.

(Some figures may appear in colour only in the online journal)

1. Introduction

Silicon avalanche photodiode (SiAPD) fabricated using a standard CMOS technology offers an efficient, ultra-sensitive, low-power, low-cost and miniaturized photodetector which can be integrated with peripheral optoelectronic circuitry on the same chip [1]. However, it is challenging to build SiAPDs using standard CMOS technology due to the lack of special fabrication steps and limitations imposed by design rules and applied CMOS process characteristics. Operating the SiAPD in Geiger mode necessitates the application of high voltage across the device. As such, there is a risk of premature breakdown of the device, particularly at the junction peripheral edges in the presence of Punch-through, high tunneling and premature edge breakdown (PEB) effects. In this case, most of the charge multiplication events will be triggered by thermal generation, which gives rise to large values of dark count and would prevent the light detection. However, a circular shape is desired for SiAPDs to reduce the possibility of corner breakdown, it might not be implantable in standard CMOS technologies because the layout rules for some standard technologies do not allow for a circular shape. The typically used solution to avoid the risk of device PEB is the implementation of a guard ring [2, 3] that generally consists in a slightly doped region (which holds higher voltage better than a heavily doped one) at the peripheral junction. It ensures high breakdown areas and reduces the electric field locally. Guard rings have been used for decades [2–5] to achieve several goals, including dark current reduction in photodiodes, $1/f$ noise reduction in oscillators, etc. Primarily a guard ring was implemented by cleaving the junction, so that only the planar junction surface remains [6]. This technique cannot be used as a standard process for a large number of pixels and cannot be included in CMOS standard processes. The diffused guard-ring technique extends the region across which the electric field develops, thereby decreasing it at the edges, but it occupies large space and lowers the fill factor [7]. In the Mesa guard ring [8], etching and subsequent filling with a dielectric physically planarizes and isolates adjacent junctions, where the fill factor and pitch are adversely impacted [8]. Another

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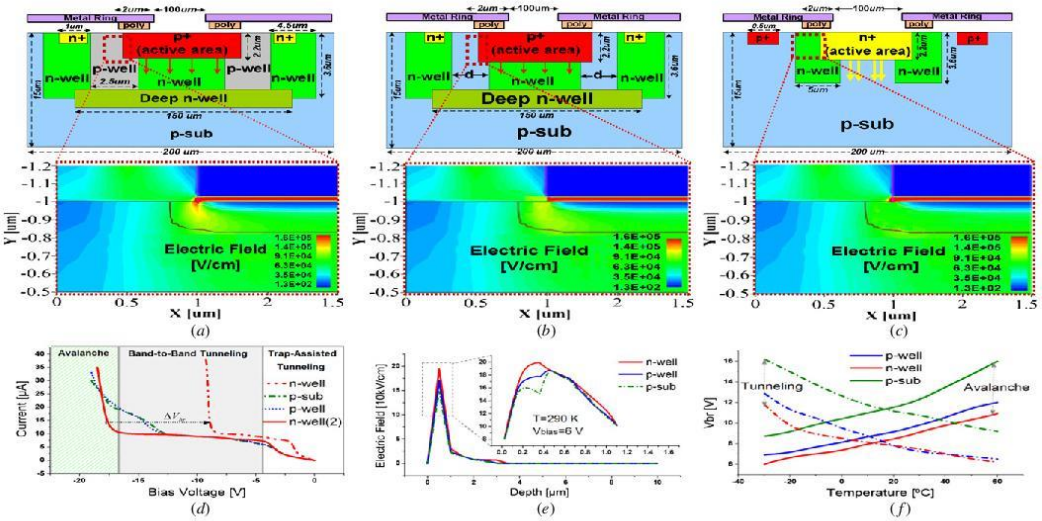

Figure 1. The cross-section and electric field distribution of p-well (*a*), p-sub (*b*) and n-well (*c*) guard-ring-based SiAPDs under the reverse bias, and their *I*–*V* characteristics(*d*) in which the n-well (2) is gained with higher doping of thicker epitaxial comparing to the n-well. The electric field profile versus depth at 6 V bias voltage (V_{br} of n-well SiAPD) in SiAPDs with zoomed electric field peak across the junction (*e*). It shows that different epitaxial layers offer different electric field distributions in the same bias voltage. The V_{br} variation at different temperatures shows whether the source of breakdown is avalanche or tunneling (*f*).

approach is to use triple-well process steps and shallow trench isolation (STI) as a guard ring to withstand the high electric fields between the anode and cathode [3]. However, STI dramatically increases the density of deep-level carrier generation centers at its interface [7]. Since the active region of the SiAPD is in direct contact with the STI, the injection of free carriers into the sensitive region of the detector results in a very high dark current rate (DCR≈1 MHz) due to the traps at the Si—SiO_2 interface and degrades the performance of an SiAPD. For some previously reported CMOS SiAPDs applied in the Geiger mode [7–11], the guard rings are realized with a p-well invariably with high DCR which limits the signal-to-noise ratio. Some of them have a buried n-type isolation layer that prevents a punch-through of the p-well guard ring to the p-substrate [1, 9, 10]. A similar guard-ring structure can also be created from the substrate doping by bringing rings of n-well into close proximity [5]. This device cannot be scaled much below 5 μm diameter because the p-well regions get so close that the active area of the SiAPD is almost fully depleted and the SiAPD performs like a planar p-well/n-well diode. Using simulation and applying different PEB prevention (PEBP) techniques however do not guarantee the functionality of SiAPDs and usually a considerable number of the dysfunctional SiAPDs are observed after fabrication [4–10]. While the impact of PEB is addressed almost in every work on SiAPD fabrication, no comprehensive and comparative study has been introduced yet. Furthermore, the role and impact of device simulation on fabrication of SiAPDs have not been addressed so far through the literature. Here we have addressed these issues, and a practical approach is proposed based on our simulation and fabrication experiences.

2. Implemented PEBP techniques in the standard process

Three SiAPD structures are proposed and implemented using relatively low-doped layers available in the standard 0.180 μm CMOS process. In order to boost the quality of the SiAPDs, we have applied a wavelength-specific design procedure. The design scales for the wavelength-specific design are gained and the guard rings are implemented on p+/n-well and n+/p-sub structures with an active area of 100 μm × 100 μm. In a p-well-based guard-ring SiAPD (p-well), the guard ring is realized by a low-doped p-well around the p+ active area of 100 μm diameter (figure 1(*a*)). In a p-substrate (p-sub)-based guard-ring SiAPD (figure 1(*b*)), no explicit guard ring is added. In other words, spacing between the active region and n-well is achieved by substrate intrinsic doping. The n-well is cleaved into two n-tubs separated by a small interval ($d \approx 0.9$ μm) constituting the guard ring. This structure is based on connecting n-wells surrounding an island of substrate as a guard ring. Deep n-wells can connect two n-wells and isolate the guard ring between the n-wells. Two separate n-wells can also be connected directly without using deep n-wells by careful positioning of doping profiles. Another implemented photodetector as shown in figure 1(*c*) is an n+/p-sub SiAPD in which the guard ring is simply developed by the n-well at the peripheral junctions (n-well SiAPD). It uses the connection between the highly doped n-well region and the substrate as the active region. The device simulations are performed using Sentaurus 3D-TCAD and Spectra imaging [1, 9] to find the best dimensions minimizing PEB. The optimal dimensions (not to scale) and current–voltage (*I*–*V*)

characteristics of the SiAPDs are shown in figures 1(*a*)–(*d*). Doping is approximately 1.25×10^{15} cm^{-3} in the p-sub, 1.28×10^{17} cm^{-3} in the n-well, 2×10^{17} cm^{-3} in the p-well and 5×10^{19} cm^{-3} in the n+ and p+ layers. The electric field distribution of the devices under reverse bias was verified as shown in figure 1(*e*). The simulation results of the electric field distributions show the maximum electric field occurring in the active regions which is a necessity for Geiger-mode operation. It shows that the maximum electric field (∼120, 160 and 750 kV cm^{-1}, respectively, for the p-well, p-sub and n-well SiAPDs) appeared in the active p+/deep n-well (n+/p-sub) junction and the devices are able to withstand the electric field without breakdown. In order to prevent the high electric field at a connection between n-wells which can cause the edge breakdown we have modified the doping profile in these regions. Small breakdown voltage (<6 V for the junction realized on mono-silicon) is more likely due to tunneling (tunneling or Zener breakdown) instead of avalanche breakdown, and the more the voltage raised, the more the leakage is due to tunneling. In order to find out if the source of the breakdown is avalanche or is due to the tunneling, we have measured the breakdown voltage variation at different temperatures [10–12]. The value of the temperature coefficient of the breakdown voltage is positive for diodes with avalanche breakdown and negative for diodes with tunneling breakdown (figure 1(*f*)). The SiAPD current as shown in figure 1(*d*) is originated from trap-assisted tunneling, band-to-band tunneling and avalanche impact ionization process, respectively, with increasing reverse bias. In order to operate an SiAPD in the Geiger mode, the transition between band-to-band tunneling and the avalanche must be sharp [13, 14]. Our experimental results show that considering only the electric field distribution does not guarantee the functionality of the SiAPD. Having a sharp transition between band-to-band tunneling and the avalanche region in *I–V* characteristics, additional to the electric field distribution will guarantee the excellent functionality of the SiAPD. However, referring to the measured *I–V* characteristics of the proposed p-well and p-sub SiAPDs (figure 1(*d*)), these structures do not show a sharp difference between tunneling and avalanche regions. Smoothness of the transition makes the Geiger-mode operation impossible using different ballast resistances as a quenching element. So these types of SiAPDs are not suitable to work as single-photon detectors.

However, the sharp transition between the band-to-band tunneling region and the avalanche region makes the n-well SiAPD suitable for the Geiger-mode operation. The general characteristics of these SiAPDs are shown in table 1. For a systematic study, 50 different chips including 100 different SiAPDs from each structure have been evaluated. The reported values in table 1 show the average of the results for functional SiAPDs. The variances of measurements for each parameter are also shown in this table. In order to examine the reliability and repeatability of the measurements, the device-to-device, wafer-to-wafer and chip-to-chip fluctuations have been verified. For example, the device-to-device fluctuations of the n-well SiAPDs are calculated as $\Delta V_{br} = \pm 1.2$ V, ΔPDP $= \pm 14\%$, Δ (dark current) $= \pm 1$ nA. The wafer-to-wafer fluctuations are calculated as $\Delta V_{br} = \pm 0.7$ V, ΔPDP $= \pm 9\%$, Δ (dark current) $= \pm 0.5$ nA, and the chip-to-chip fluctuations are calculated as $\Delta V_{br} = \pm 1$ V, ΔPDP $= \pm 10\%$, Δ (dark current) $= \pm 1.3$ nA. The proposed SiAPDs were also studied with STI guard ring. However, due to their significant DCR degradation (as shown in table 1) they were not considered further for fabrication. It is also notable that a significant discrepancy in photon detection probability (PDP) and noise factor (*F*) at a specific multiplication gain (*F@M*) was observed in simulation using TCAD (or spectra) and 3D TCAD (separated by a slash in table 1). The discrepancy between simulation and measurement results are due to the fixed doping concentrations for layers in the standard CMOS process, effects of the used bonding pad parasitic capacitance and also the passivation layer imposed by fabrication on the performance of the designed SiAPDs. Among the three families of structures (p-well, p-substrate and n-well guard ring), only the SiAPD with an n-well-based guard-ring structure could be biased in the Geiger mode, because the other structures suffer from drawbacks such as punch-through, high tunneling and PEB. For more characterization and comparison of the proposed structures, their PDP in different wavelengths, their PDP variation in different excess bias voltages, their V_{br} variation (with respect to the V_{br} at nominal thickness) as a function of absolute reduction/increment in the epitaxial layer thickness, and their *F–M* relationship at 650 nm are shown in figures 2(*a*), (*b*), (*c*) and (*d*), respectively. Because of the considerably better performance offered by the n-well SiAPD compared to other devices, here we have characterized it in detail. The electric field distribution strength in the cross-section of the n-well SiAPD at different depths in the absence of any radiation is depicted in figure 3(*a*). It shows that the n-well guard ring is mostly effective near the surface of the SiAPD, where most of the photon absorption takes place and the maximum electric field (∼750 kV cm^{-1}) is in the active region, so the device is able to endure the electric field without breakdown. Figure 3(*b*) shows the DCR in different excess bias voltages. In order to avoid high DCR, the excess bias (V_{ex}) has to be kept low enough at the cost of having a lower photon detection probability. A decrease in the excess noise factor with increasing doping concentration or decreasing device length was observed. The n-well SiAPD offers a relatively low dark current (<∼100 nA) generated by tunneling and Shockley–Read–Hall (SRH) processes. The SRH process is strongly proportional to temperature variation comparing to the respectively weak and inverse dependence of tunneling and after-pulsing (post-pulsing). The SRH and tunneling are both voltage and temperature dependent, however, the SRH dependency to temparature is much stronger compared to tunneling. The SRH dark count is dominated in temperatures higher than a specific value, while below that temperature value the tunneling is dominated and may impose a slight increase in power consumption at high illuminations [14]. So it is possible to distinguish between dark counts originated from SRH process or tunneling. STI formation is known to introduce defects and crystal lattice stresses which cause high DCR. So it is normally important to move the trench away from the main SiAPD p–n junction. Poly-silicon (using a poly-ring around the periphery defining a thin oxide region) is applied to prevent

Table 1. Main specifications of the proposed SiAPDs (Area = 100 × 100 μm^2).

APD	Data source	Gain (M)	PDE @ 700 nm	Impedance (Ω)	Capacitance	F @ $M = 20$	Breakdown voltage (V)	DCR	Functional SiAPDs (%)
No GR	Simulation	40	9%	20	2 pF	93	18	670 kHz@$V_{ex} = 2$ V	–
	Measurement	35 ± 4	6% ± 2%	28 ± 1.5	4.5 ± 0.01 pF	95 ± 6	18 ± 3	670 ± 20 kHz@$V_{ex} = 2$ V	63
p-well	Simulation	100	25%/21%	600	1 pF	70/79	12	100 kHz@$V_{ex} = 1.7$ V	–
	Measurement	100 ± 6	24% ± 1%	630 ± 3.7	1 ± 0.00 pF	83 ± 1	12 ± 3.5	100 ± 1 kHz@$V_{ex} = 1.7$ V	76
p-well+STI	Simulation	100	25%/21%	600	1 pF	70/79	12	140 kHz@$V_{ex} = 1.7$ V	–
p-sub	Simulation	200	20%/18%	0.5	1 pF	50/59	9	4 kHz@$V_{ex} = 1$V	–
	Measurement	200 ± 10	20% ± 2%	0.8 ± 0.18	1.3 ± 0.1 pF	61 ± 0.1	9 ± 3.1	4 ± 1 KHz@$V_{ex} = 1$ V	67
p-sub+STI	Simulation	200	20%/18%	0.5	1 pF	50/59	9	7 kHz @ $V_{ex} = 1$ V	–
n-well	Simulation	800	85%/70%	0.5	0.5 pF	36/40	6	40 Hz @ $V_{ex} = 1$ V	–
	Measurement	800 ± 5	70 ± 2%	0.5 ± 0.02	0.6 ± 0.03 pF	41 ± 0.01	6 ± 2	40 ± 4 Hz @ $V_{ex} = 1$V	91
n-well+STI	Simulation	800	85%/70%	0.5	0.5 pF	36/40	6	1 kHz@ $V_{ex} = 1$ V	–

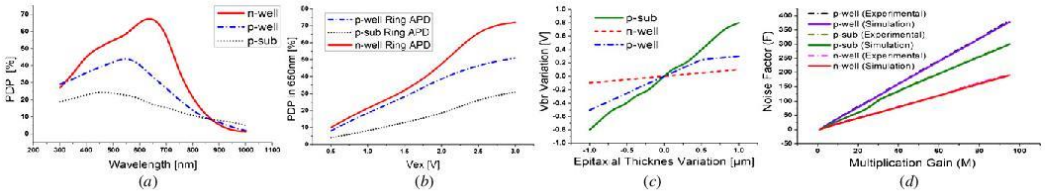

Figure 2. PDP of the proposed SiAPDs at room temperature (*a*) and their PDP variation with different excess bias voltages (*b*). The ΔV_{br} (with respect to the V_{br} at nominal thickness) as a function of absolute reduction/increment in the epitaxial layer thickness in different SiAPDs (*c*) and the *F*–*M* plot at 650 nm (*d*).

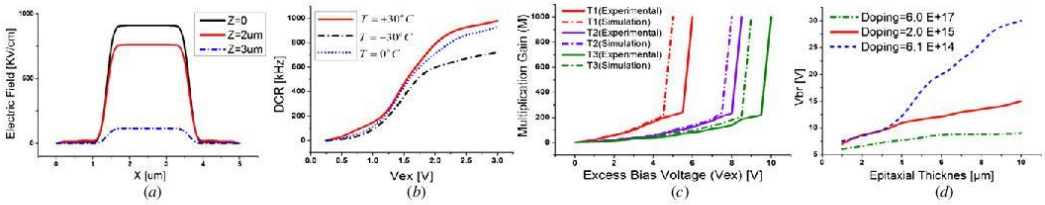

Figure 3. The n-well guard-ring-based SiAPD characterization: the electric field distribution (*a*), DCR-V_{ex} variation (*b*). The *M*–*V* plot in different temperatures where $T_1 = -25$ °C, $T_2 = -25$ °C, $T_3 = 25$ °C (*c*) and the TCAD simulated V_{br} dependence on the epitaxial layer thickness in different epitaxial p-type doping (*d*).

STI creation near the active region and to move STI out of the active region. It also reduces the after-pulsing significantly [2, 10]. Using poly-gate in the proposed guard rings where no STI is implemented, we still observe a significantly lower DCR (∼50%) accompanied by a trivial reduction in sensitivity as shown in table 1. This may be due to the partial transparency and low transmittance of poly-silicon at short wavelengths. The poly-gate has a suitable structure to accumulate and transfer carriers. Biasing the poly-silicon layers on top of the SiAPD produces a depletion region which acts as an accumulation region for photo-generated carriers and it can also increase the lifetime of the SiAPD. The *M*–*V* characteristics of the n-well SiAPD in different temperatures are also depicted in figure 3(*c*). High tunneling is expected in high V_{ex} values due to the applied relatively highly doped substrate in this SiAPD. We have examined the effect of doping and scale variations in order to optimize the SiAPD performance. While the breakdown voltage is reduced in higher CMOS technologies due to the higher doping levels, the noise also becomes generally lower. One of the reasons is that the ionization coefficient ratio (k) is closer to unity, so the noise due to electron–hole-initiated avalanche is lower. However, with downscaling of technology, the dark current increases.

This is due to the increase in the doping concentration which increases the emission rate of carriers from traps in SiAPD structure and also higher gate leakage current in 0.18 μm and technologies below it. Furthermore, the quantum efficiency is also reduced due to the reduction of the absorption-region depth and an increase of the dark current due to the contribution of tunneling. However, the thickness of the n-well is constrained by design rules; our investigations based on the simulated and implemented structures show that the thicker and deeper guard rings show better performance as depicted in figure 3(*d*). The high doping values and shallow depths imposed by the applied technology constrain the technical design to reach desired high detection efficiency.

3. Conclusion

The impact of PEB and the most efficient PEBP techniques in CMOS silicon avalanche photodiode design and fabrication are addressed and evaluated in this paper followed by the design, simulation and fabrication of three proposed techniques. Inefficiency of the applied PEBP techniques and corresponding device simulations can lead to a low performance or dysfunctional SiAPD and also significant discrepancy between simulation and measurement characteristics. In addition to the doping profile and electric field distribution in an SiAPD structure, the punch-through, high-tunneling and PEB effects should be considered to design a high-quality SiAPD using the standard CMOS process. The sharpness of the transition between band-to-band tunneling and the avalanche has to be considered as a critical design criterion. By implementing different SiAPD structures, we studied the geometric trade-offs involved in the design of deep-submicron SiAPDs. The p-well and p-substrate structures suffer from punch-through, high tunneling and PEB. However, the SiAPD with the n-well-based guard-ring structure offers the highest sensitivity and PDP-to-DCR ratio characteristics and could be biased properly in the Geiger mode.

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APPENDIX 3 – PAPER #2

Low-Noise, High-Gain Transimpedance Amplifier Integrated With SiAPD for Low-Intensity Near-Infrared Light Detection

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Low-Noise, High-Gain Transimpedance Amplifier Integrated With SiAPD for Low-Intensity Near-Infrared Light Detection

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***Abstract*— A fully integrated near-infrared spectroscopy photoreceiver including two new silicon avalanche photodiodes (SiAPDs) and a new transimpedance amplifier (TIA) is proposed in this paper. SiAPDs are designed in p+/n-well structure with guard-rings realized in different shapes. The TIA front-end has been designed using distributed-gain concept combined with resistive-feedback and common-gate topology to reach low-noise, low-power consumption, high gain-bandwidth product characteristics and it is robust against power-supply variation (1–3 V). This circuit is developed using 0.35 μm CMOS technology and the measurement results are compared with other results from the literature. The designed rectangular and octagonal SiAPDs have the avalanche gain of 100 and 45 with the breakdown voltage of 9 and 6 V and the photon absorption efficiency of 45% and 25% at 800 nm. Fabricated TIA offers high-transimpedance gain (up to 250 MV/A), tunable BW (1 kHz–1 GHz), extremely low input and output noises (100 fA/$\sqrt{}$Hz, 1.8 μV/$\sqrt{}$Hz), and low-power consumption (0.8 mW). The impact and effects of on-chip integration of SiAPD and TIA front-end have been also measured and evaluated.**

***Index Terms*— Avalanche photodiode, CMOS photoreceiver, medical imaging, fNIRS, transimpedance amplifier.**

I. Introduction

CLINICAL functional near-infrared spectroreflectometry (fNIRS) is a non-invasive, minimally intrusive, safe, and high-temporal resolution imaging technique for real-time monitoring of the brain function and biological tissues. It is currently considered as an efficient technique for the evaluation of different neurological diseases, such as stroke and epilepsy seizures that requires continuous monitoring of the patient at the hospital [1]. fNIRS measures information on cerebral oxygenation and blood volume at low-cost. In fNIRS, light is injected into the brain tissue and the backscattered signal is observed to investigate the brain function (Fig.1). The brain tissue is a highly scattering tissue with high diffusion. However in the NIR region of the electromagnetic spectrum (650nm-950nm), water has relatively low absorption while oxy- and deoxy-hemoglobin dominate absorption. Lower absorption and diffusion allow photons to propagate over centimeters enabling imaging of brain tissues [2]. Continuous-wave fNIRS (CW-fNIRS) systems use continuous light to measure the attenuation in amplitude of the incident light. Relative concentration changes in chromophores can be computed according to the Beer–Lambert law. The first interface with the human body and the main building block of an fNIRS system is the photo-transceiver front-end. The block diagram of a typical CW-fNIRS phototransceiver is depicted in Fig. 1. It includes NIR light source(s) and detector(s). The light source is placed on the surface of the head (scalp). In CW systems they can be either laser or light emitting diodes (LEDs) that emit NIR light with optical power within a range of 5mW to 17mW at discrete wavelengths [3]. Using LEDs increase the safety and lead to a more cheap and compact instrument to be applied for clinical and educational applications [4]. The sensor is a photodetector that monitors the intensity of the backscattered NIR signal. As the first stage of any optical receiver is a photodiode which converts the incident photon density into a current signal, the first block of the photoreceiver in this case is a TIA. Work is currently being performed in different research groups to improve the performance of NIRS system [4], [5]. While fNIRS is compact compared to other brain imaging systems, current commercially available NIRS devices remain too bulky to be wearable or portable. However some wireless devices have been proposed for portable near-infrared spectroscopy [2], [6], they are not miniaturized enough in order to easily be integrated with other medical

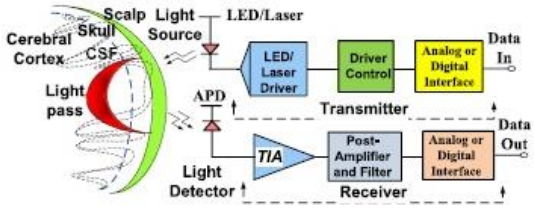

Fig. 1. Banana-shaped detected photon path of fNIRS and the block diagram of a typical CW- fNIRS Phototransceiver front-end.

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imaging systems such as electroencephalogram (EEG) or to be used as a wireless and portable device for bedside real-time brain monitoring. So developing a more compact system is required for real-time and portable brain imaging using fNIRS. The main components of fNIRS photodetector front-end are the photodiode and the amplifier. The photodiode used in the photodetector requires being highly sensitive, enabling the reliable conversion of the ultra-low amplitude light signal into a detectable electric signal. Conventional photodetectors use photon multiplier tubes (PMTs) which are bulky, sensitive to magnetic fields and require high-voltage supply [7]. Silicon avalanche photodiode (SiAPD) is a candidate for low-level light detection in the visible and near-infrared regions due to its bias dependent internal gain and its ability to amplify the photogenerated signal by avalanche multiplication [18]. APDs have been commercially available for more than 30 years normally with a dedicated process, which do not allow monolithic integration with other electronic circuitry [10]. A critical element for NIRS front-end receiver is to design a low-noise and sensitive photodetector to ensure maximum detection of the reflected NIR light that is strongly attenuated (7-9 orders of magnitude) by the biological tissues. A minimal signal-to-noise ratio (SNR) of ~40 dB is needed for NIRS application. SiAPDs with dark current in nA range, and the generated photocurrent in hundreds of μA range confirms SNR of much higher than 40dB [3], [9]. But no photodetector with these necessary specifications has been reported in the literature yet. A miniaturized, low-noise and high-gain CMOS photodiode with high detection efficiency and low-breakdown voltage is proposed in this paper using standard CMOS technology. It is developed using p+/n-well topology with guard-ring realized by low-doped p-well around p+ active area and low-doped n-ring using relatively low-doped layers available in standard 0.35μm CMOS technology.

In order to design a continuous-wave fNIRS photodetector front-end we have introduced several front-ends and reported their simulated characteristics in [28] as proper candidates to be integrated with the SiAPD on the same chip. The goal was to develop a compact and cost-effective photodiode and other electronic circuits of a NIRS front-end receiver on the same chip using standard CMOS process. In recent years, work in this direction has been demonstrated [10], [11]. There are mainly three Photoreceiver-TIA structures reported in literature: common-gate TIA, resistive feedback TIA, and capacitive feedback TIA. Common-gate TIA (CG-TIA), usually used in open-loop topology and exhibits low-input impedance and high-transimpedance gain, however its input noise current and input bias current are high and its BW is also low. In resistive-feedback TIA (RF-TIA), the transimpedance gain is high and offers the smallest noise specially at high frequencies comparing to other structures, but its BW is limited. Capacitive-feedback TIA (CF-TIA) offers lower noise at low frequencies but it is noisy at higher frequencies. A common-gate configuration is typically chosen as it can tolerate a wide range of SiAPD capacitance. However, resistive feedback architecture has better noise performance and is more attractive when SiAPD models are readily available. Reported amplifiers for this case [35], [38] are suffering from several limitations so that trade-off between necessary parameters occurs with the cost of losing reliability and performance. For example reported variable-gain transimpedance amplifiers are difficult to stabilize [39], [40]. The key problem with these designs is that they are based on the traditional two-stage topology consisting of a common-source gain stage followed by an output buffer [41], [42]. By combining a common-gate and resistive-feedback TIA topologies based on dynamic-threshold voltage MOSFET (DTMOS), and using distributed gain concept, we have designed an integrated low-noise, high-gain and low-power photodetector amplifier for fNIRS imaging. The proposed APDs and their characteristics are presented in section II. In section III the new proposed TIA front-end is introduced and the characteristics of the fabricated integrated circuit are presented. Finally the impact and characteristics of the integrated APD+TIA are explained in section IV.

II. CMOS Photodetector Design

A. Background and Design Requirements

The main design parameters of SiAPD include area, depletion region thickness, sensitivity, quantum efficiency, SNR, fabrication technology and architecture. The SiAPDs fabricated using dedicated process have two major drawbacks: their production cost is too high due to the specialized fabrication process, and it is unfeasible to integrate them with electronic circuits on the same chip. Optimizing the performance of both the CMOS devices and the SiAPD is a non-trivial job. To overcome these problems, researchers have investigated the design and fabrication of SiAPDs in standard CMOS process [22]. The advantages of standard CMOS fabrication process are: the availability of a fully supported, mature and reliable technology at reasonably low-cost, and the possibility of developing a complete system on chip with a high degree of complexity [9], [22]. The mandatory requirement for SiAPD fabrication in standard CMOS process is that a suitable subset of CMOS fabrication process flow should be able to build a planar p-n junction without device breakdown at the photodiode periphery [23]. SiAPD fabricated using standard CMOS process involves high-doped p or n layer resulting in shallow or medium depth depletion region. However, to increase the use of SiAPD-based front-end receivers for biomedical applications, integration of the SiAPD and peripheral circuitry on the same chip using standard CMOS technology is highly desired.

It is challenging to make SiAPDs in standard CMOS technology due to lack of special fabrication steps. Several research groups have fabricated SiAPDs using standard CMOS technology [24], [25]. The area and design of the SiAPDs for different CMOS technologies are different which result in a wide range of performance. Photon detection efficiency is better for larger area SiAPDs, but larger area can be more suitably designed using older CMOS technology. Use of older CMOS technology will increases area and power consumption for the rest of the electronic circuits of the NIRS front-end receiver. On the other hand, doping concentration levels in CMOS increases as the technology advances, causing an

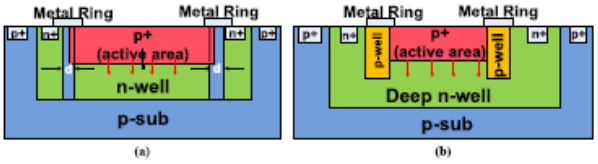

Fig. 2. The cross-sectional view of the proposed APD1 (a) and APD2 (b).

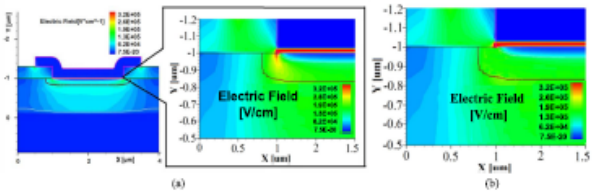

Fig. 3. Device simulation of the APD2 under reverse bias using TCAD.

TABLE I
ESTIMATED CHARACTERISTICS OF THE TSMC CMOS 0.35-μm TECHNOLOGY

Layer	Depth (μm)	Doping (cm^-3)
P-Sub	-	1.27×10^15
N-Well	1.25	1.25×10^17
P-Well	1.28	2.01×10^17
N+ Contact	0.24	5.01×10^19
P+ Contact	0.23	5.02×10^19

increase in the peak electric field in the depletion region and decrease in the breakdown voltage of the diodes. Advanced CMOS technology can yield SiAPDs with low-breakdown voltage ensuring safer operating condition for biomedical applications [25]. Due to the low-level of detected light in fNIRS, the area of the photodetector should be large enough so that it can capture enough optical photon to generate detectable electric signal. Earlier silicon p-i-n photodiodes were successfully used for NIRS systems with an active area of ~7.5 mm^2 [3]. SiAPDs are also commercially available with comparable active area and are being used in several NIRS systems (e.g. Hamamatsu C5460-01 device 7 mm^2). However, these commercial SiAPDs necessitate a dedicated fabrication process, and cannot be fabricated on the same chip with the rest of the front-end circuit. On the other hand, the performance of SiAPDs fabricated using standard CMOS process degrades with area size which limits their active area to 0.003 mm^2 [3], [9]. Recent progresses in the standard CMOS fabrication process allow producing SiAPDs with active area of up to 0.3 mm^2 (~200 μm diameter) while maintaining adequate performance. Again, the higher the thickness of depletion region of SiAPD, the better is its photon absorption efficiency. However, a thick depletion region increases the noise of the SiAPD. To ensure reasonable amount of photon absorption (~70%) in NIR range, it is of primary importance to design SiAPDs with at least 10 μm thick depletion region [3], [22].

B. New integrated CMOS APD

Here, we propose a new SiAPD structure based on the previously proposed structures in [26] and [27] using relatively low-doped layers available in standard 0.35μm CMOS technology. These APD structures have been simulated and characterized previously at [3], [28], [29]. However a circular shape is desired for APDs to reduce the possibility of corner breakdown [24], [30], the layout rules for the technology do not allow for a circular shape. Here we have designed the p+/n-well SiAPDs with guard-ring in two different square and octagonal shapes. These provide a trade-off between fill-factor (FF) and angularity and a feasible way to validate the efficiency of the applied guard-rings. Schematic of the cross-section and plan view (not to scale) of the first proposed CMOS SiAPD (APD1) are depicted in Fig. 2(a). It is a square shape p+/n-well avalanche photodiode with guard-ring. The guard-ring is realized by low-doped n-ring due to n-wells lateral diffusion [24]. The n-well is splitted into two n-tubs separated by a small p-sub interval (d≈0.9μm) constituting the guard-ring. We have developed this APD with two different active areas of 100μm×100μm and 400μm×400μm. The second APD (APD2) is also a p+/n-well APD developed in square and octagonal shape (with active area of 100μm×100μm) with guard-ring to preventing premature edge breakdown. The guard-ring is realized by low-doped p-well around p+ active area with 100μm diameter (Fig. 2(b)). Optimization of the performance of SiAPD is done by device level simulation using Sentaurus TCAD software. The active junction of the photodiode exists between p+ (Na=5×10^{19}/cm^3) and deep n-well (Nd=1.28×10^{17}/cm^3). The doping concentrations for these layers are fixed for 0.35μm CMOS technology. We created the masks for the SiAPD structure using Ligament Layout Editor and created an input command file for Ligament Flow Editor. The input command file emulates the fabrication process and creates the structure and its doping data. The output from Ligament Flow Editor serves as an input for Sentaurus Process, which produces doping profile and electric field distribution of the APD. Fig. 3 shows the electric field distribution of the APD2 device under reverse bias. Fig. 3 (a) shows the device simulation of the APD2 structure without efficient guard-ring. It shows a premature edge breakdown (high electric field in the periphery of the device), so it will not function as an efficient APD. The avalanche without edge breakdown is shown in Fig. 3 (b). It shows that the maximum electric field (~10^{5}V/cm) appeared in the active p+-deep n-well junction and the device is able to withstand the electric field without breakdown. One of the main difficulties for optimal CMOS APD design and fabrication is the technological constraints imposed by CMOS chip manufactures (e.g. AMS, IBM and TSMC). Manufactures do not give out doping profile information for their technologies. Referring to the applied technology layers doping and depth characteristics, we can point out the weak depths and the high doping values applied in the technology. For example Table I shows the main characteristics for TSMC CMOS 0.35-μm technology. The general specifications of the developed APDs are shown at Table II. The values which are based on TCAD simulation are somewhat unrealistic. For example in contrast to the gained photon detection efficiency (PDE) values, in general

TABLE II

DESIGN SPECIFICATIONS OF THE PROPOSED SIAPDS AND COMPARISON WITH DIFFERENT SiAPDS

Reference / Parameter	[7]	[8]	[19]	[21], [23]	[24]	[26]	[27]	[31]	[33]	This work							
										APD1				APD2			
										Rectangular (Simulation)	Rectangular	Rectangular (Simulation)	Rectangular	Rectangular (Simulation)	Rectangular	Octagonal (Simulation)	Octagonal
CMOS Tech.(μm)	0.35 (HV)	0.13	0.7 (HV)	0.8 (HV)	0.18	0.8	0.35	2 (BiCMOS)	0.8	0.35	0.35	0.35	0.35	0.35	0.35	0.35	0.35
Type	p-/n-	P+/n-well	n+/p-sub	n+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well
Guard-Ring	p-tub	p-well	-	p-tub	p-well	p-well	p-well	p-base	p-tub	n-tub	n-tub	n-tub	n-tub	p-well	p-well	p-well	p-well
LinearGain	–	–	10–40	–	-	23	20	15	<150	103	20	100	100	200	45	100	15
Area (μm)	Circula r:5μm diam.	Octagonal :10μm diam.	Circular:2 5-800μm diam.	Circular: 12μm diam.	Octagonal :10μm diam.	80×80	100×100	2	28×28	100×100	100×100	400×400	400×400	100 ×100	100 ×100	100×100	100×100
PDE (QE%)	5% @ 840nm	5%@ 800 nm	20%@ 800nm	0.5%@ 950nm	1%@ 700 nm	50%@ 470nm	23%@ 480nm	40%@ 500nm	50%@ 550nm	35% @800nm	5% @800nm	48% @ 800nm	45% @ 800nm	55% @ 800nm	25% @ 800nm	37% @ 800nm	2% @ 800nm
V_{BR}	35 V	10 V	12 V	55 V	10.2V	19.5V	10.8V	42 V	25V	9 V	9 V	9 V	9 V	6 V	6 V	6 V	6 V
F@M=20	-	-	30@ 650nm	-	-	7@ 400nm	6@ 560nm	36000@ 635nm	50@ 470nm	74@ 800nm	74@ 800nm	50@ 800nm	50@ 800nm	60@ 800nm	60@ 800nm	150@ 800nm	150@ 800nm
Impedance	-	-	-	-	-	-	-	-	-	600 Ω	1 kΩ	600 Ω	620 Ω	0.5 Ω	0.6 Ω	0.5 Ω	1.3kΩ
Capacitance	-	-	-	-	-	-	-	-	-	1pF	630 pF	32pF	34pF	1pF	1pF	1pF	0.8nF

the Photodiodes implemented in standard CMOS will rarely have peak PDE >70% due to losses in the optical stack, unless using backside illumination and antireflection top coating or adopting a CMOS image sensor [9]. For the measurements, we have coupled a light source through a 1μm fiber optic and illuminated the detector by positioning the fiber on top of the APD. The PDE is defined as:

$$PDE = \frac{C_R - I_{dark}}{N} \approx \frac{I_{ph}}{P_{ph}} . \frac{1.24 \times 10^{-6}}{\lambda} \quad (1)$$

where I_{ph} is photocurrent, P_{ph} is the incident optical power and λ is the wavelength of the incident light. PDE can be calculated by measuring the count-rate (C_R) at a certain incoming photon rate $N = P\lambda/hc$, where P is continuous-wave (CW) optical power focused in a spot in the middle of the APD photosensitive area, λ is the wavelength of the incident light, h is the Planck's constant, and c is the speed of light. The optical power illuminating the detector $P = P_1 \times 10^{(-a/10)}$ is obtained by measuring CW light power (P_1) with an optical power meter, then attenuating the light down to single-photon level with a set of calibrated attenuators (variable attenuator and neutral density filters) providing a cumulative attenuation. We remark that PDE could be further increased slightly by decapsulating the APD package, whose entrance window is not antireflection coated [57]. Although the efficiency of the designed APDs verified accurately by simulation, but as we expected before, there was a discrepancy between the simulated and measured parameters, especially regarding to the PDE, and dark current of the fabricated APDs. This is due to the inflexibility of the standard CMOS technology regarding to the precise simulation and implementation of the considered characteristics. The doping concentrations for layers are fixed for 0.35μm CMOS technology, so implementation of the predefined optimal doping profiles (extracted from analytical calculation and simulation) is not possible precisely. The other source of this mismatch can be due to effects of the used bonding pad parasitic capacitance and the passivation layer imposed by fabrication on the performance of the designed APDs. It also might be due to the limited accuracy of the test setup used to get these values or the inadequacy of the applied device simulation tool. The APD2 showed a significantly lower current in dark condition comparing to APD1. This can be due to the implemented highly doped n-well (deep n-well) in this structure which reduces the substrate leakage noise and reduces the dark current. The output impedance of the SiAPD should be considered for impedance-matching with the integrated front-end amplifier. The output impedance of APD2 under reverse bias was around 0.5Ω and for the APD1 was around 600Ω. The capacitance of the photodetector increases with its area with measured values being 1pF for a $100\mu m^2$ SiAPD and 32 pF for $400\mu m^2$ SiAPD. The V_{br} has been defined as the bias voltage on the reverse I-V characteristic at which the second derivative of the logarithm of the current has its maximum. The values found with this method [58], [59] correspond to the ones extrapolated from the M-V plot (Fig. 4(c)). For APD1 and APD2, the breakdown happened at approximately 6V and 9 V respectively. The APD2 with no guard-ring does not have a sharp breakdown profile, indicating that edge breakdown is occurring. The APD current is originated from trap-assisted tunneling, band-to-band tunneling and avalanche impact ionization process respectively, with increasing reverse bias. In order to operate an APD in Geiger mode the transition between band-to-band tunneling and the avalanche must be sharp. Small breakdown voltage (<6 V for the junction realised on mono-silicon) is more likely due to the tunnelling (Tunnelling or Zener breakdown) instead of avalanche breakdown and the more the voltage is raised, the more leakage is due to tunnelling. In order to find out if the source of the breakdown is avalanche or it is due to the tunnelling (which limits the sensitivity of the APDs), we have measured the breakdown variation in different temperatures. The breakdown voltage of SiAPDs at temperature T is equal to:

$$V_{br} = V_{bias}[1 + \beta(T - T_0)] \quad (2)$$

The value of β (temperature coefficient of the breakdown voltage) is positive for diodes with avalanche breakdown and negative for diodes with tunnelling breakdown [9], [24]. The negative value of β shows that the breakdown mechanism of our diode is indeed tunnelling. The Figs. 4(a)-(b) shows

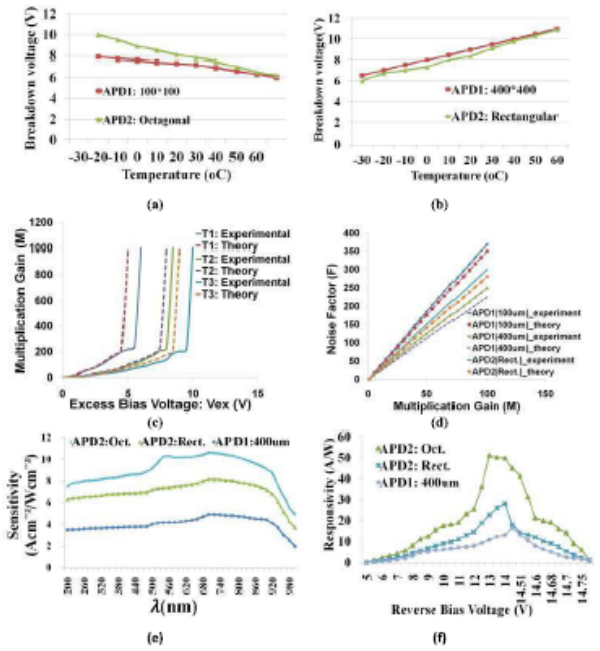

Fig. 4. Breakdown voltage variation in different temperatures: The breakdown due to tunneling (a) and avalanche (b). The M-V plot in different temperatures where T1=–25°C, T2=25°C, T3=75°C (c) and the F-M relationship while λ =800nm (d). The spectral sensitivities of APDs (e) and Measured responsivity as a function of applied reverse bias voltage (f).

the breakdown voltage variation with temperatures for different APDs. For cooling and evaluation of APD in different temperatures, it has been mounted on a thermoelectric cooler (TEC) as introduced in [57]. 3-stage and 4-stage TECs also can be used for lower temperatures. In order to reduce the heat flow via air convection, the TEC-APD assembly was tightly surrounded with cut-to-shape styrofoam. Referring to the Figs. 4(a)-(b), the octagonal shape APD works in normal mode, not in avalanche mode and more investigations showed that it is mainly due to effects of the bonding pad parasitic capacitance on the measurements. The general specifications of the proposed APDs are summarized in Table II. It is also includes the comparison of the proposed APDs with other works. The APD multiplication gain (M) is a critical requirement for APDs due to the high background and detector noise. It is calculated using following formula:

$$M = 1/(1 - \int_0^L \alpha(x)dx) = 1/(1 - (\frac{V}{V_{br}})^n) \quad (3)$$

where L is the space charge boundary for electrons and α is the multiplication coefficient for electrons (and holes), strongly depended on the applied electric field strength, temperature, and doping profile. The linear gain (M) is characterized using dark current and photocurrent values. The dark current present when no signal impinges the APD, must be subtracted from the measurement for proper gain calculation. The gain is defined as the ratio of the current measured at a given bias voltage to the current measured at a specific voltage (V1<Vbr). We have considered V1=6V, 5V for APD1 and APD2 respectively. The relationship between multiplication gain and bias voltage of APD1 (400μm) is depicted in Fig. 4(c). It also compares the theoretical and experimental relations. It is obvious that the multiplication gain predicted by Equation 3 is better than one gained by the experiment. This shows the gain is overestimated using this formula. Avalanche noise is measured in terms of excess noise (F). The excess noise with pure hole injection (F_h) is equal to:

$$F_h(M) = M\frac{\alpha_n}{\alpha_p} + (2 - \frac{1}{M})(1 - \frac{\alpha_n}{\alpha_p}) \quad (4)$$

where M is the multiplication factor, α_n and α_p are the electron and hole ionization coefficients for the material [31], [32]. This equation has been plotted in Fig. 4(d) and compared with the experimental values. It shows the noise values are somehow underestimated using this equation. In table II, the F@M=20 indicates the noise factor value (F) at specific multiplication gain of 20 (M=20). For the wavelength specific applications also the spectral sensitivity of the detector should be considered. The sensitivity is calculated as the photocurrent per unit area of the photodiode for a given irradiance. The sensitivity of a PIN photodiode based optical receiver, as shown for the proposed APDs in Fig. 4(e), is given by [53]:

$$S = \frac{Q}{R}(qQB + \sigma_T) = \frac{\lambda \times Q_e}{1240} \times 100\ (\%) \quad (5)$$

where S is sensitivity (W), Q_e is the quantum efficiency, Q is desired Q-factor (related to the desired bit error rate or BER), R is the photodiode responsivity (A/W), q is charge of an electron (C), B is receiver bandwidth (Hz) and σ_T is the rms thermal noise current (A) and is given by:

$$\sigma_T^2 = (4k_BT/R_L)\ F_nB \quad (6)$$

where k_B is Boltzmann's constant (W/°K), T is temperature (°K), R_L is the receiver load resistance (Ω) and F_n is the receiver noise factor. The photoreceiver sensitivity depends on its quantum efficiency, the light source power, target reflectivity, environmental conditions, receiver optical design, and amplifiers noise. Low excess-noise, large active-area, and high-speed APDs improve the sensitivity of the Photoreceiver front-end and consequently allows the use of low-power light source to reduce the power consumption and cost. However, the Photodetector dark currents and capacitance increase with the active area and have adverse effect on receiver sensitivity and bandwidth. The Photodetector BW is also limited by the RC effect in large active area APDs and special efforts are needed to reduce APD capacitance while maintains the same active area [62]. The measured sensitivity has been normalized to the same BW, BER, wavelength and bit-rate for all devices. The APDs with lower sensitivity, require higher-gain TIAs, limiting amplifiers and adaptive equalization. The challenge was amplification with low thermal-noise, while ensuring a high front-end BW [63]. The modulation frequency (~100Hz-100MHz) is critical for the choice of bandwidth of the front end amplifier which determines the sensitivity of the instrument [64]. The proposed SiAPDs offer small junction/parasitic capacitances, and consequently high-BW and low-noise front-ends. "Higher sensitivity may be achieved by adding an

anti-reflection coating, improving the optical collection as well as the residual flux filtering [65]. Responsivity of the APD characterizes the performance in terms of the generated photocurrent I_{ph} per incident optical power P_{opt} at a given wavelength and is:

$$\Re = \frac{P_{ph}}{P_{opt}} = \frac{\eta \,.\, q}{h \,.\, \upsilon} = \frac{\eta\, \lambda\, (\mu m)}{1.24} \quad [\frac{A}{W}] \tag{7}$$

The Responsivity of the proposed APDs is shown in Fig. 4(f). It shows that the maximum responsivity of the proposed APDs is at reverse bias voltage of ~13-14V.

III. CMOS TIA Front-End Design

A. Background and Design Requirements

The optical preamplifier interfacing the photodiode to the rest of the receiver plays a crucial role in determining many aspects of the overall performance of the receiver including speed, sensitivity, and dynamic range. For linear-mode operation, SiAPDs require a transimpedance amplifier (TIA) to convert the input photocurrent into a voltage signal [34]. Due to the ultra-low level and usually high-source impedance of the photodiode, the amplifier has to meet certain basic requirements. The basic requirements in designing a proper TIA for portable fNIRS systems are: High Common Mode Rejection Ratio (CMRR) to reject interference from mains and boost the SNR, HPF characteristics for filtering differential DC offset, low input-noise (<1 nA) for high signal quality, ultra-low power dissipation (<50 mW) for long-term power autonomy, configurable gain and filter characteristics that suit the needs of different biopotential signals and different applications, high transimpedance gain (>1 k), narrow Bandwidth (around 100k), high output swing and low-voltage operation [34]–[37]. Work on developing such photoreceiver amplifier has not been considered in the literature yet and none of the reported NIRS detectors offer these features all together in a single design, which is a crucial factor in real- time brain imaging. Phang et al. [39] have proposed a TIA by combining a sub 1-V current mirror [40] and a common-gate TIA [41] based on a current-gain amplifier for optical communication. Achigui et al. [5] modified this TIA by adding an Operational Transconductance Amplifier (OTA) with DTMOS for NIRS front-end photoreceiver. These designs all are based on fixed-gain and only one mode of operation. Reaching high data-rate and high-BW in these designs is also with the cost of small gain, high-noise and power consumption. So the need for a new design with the ability to overcome these limitations and meet the requirements of a fNIRS photodetector front-end is a critical issue we aim to solve. Because of the inverse dependency of gain and bandwidth (BW) in a single-stage amplifier, designing a single-stage amplifier with high GBW is a challenging task. If the GBW of each amplifying stage is constant, then the time-constant for an N-stage amplifier with identical gains per stage is proportional to $\sqrt[N]{N}\sqrt{A}$, while it is proportional to A for a single-stage amplifier [29], [42]. So a cascade amplifier has a significantly larger GBW than a single-stage amplifier with the same gain. Using distributed gain (DG) amplification and adaptive feedback it

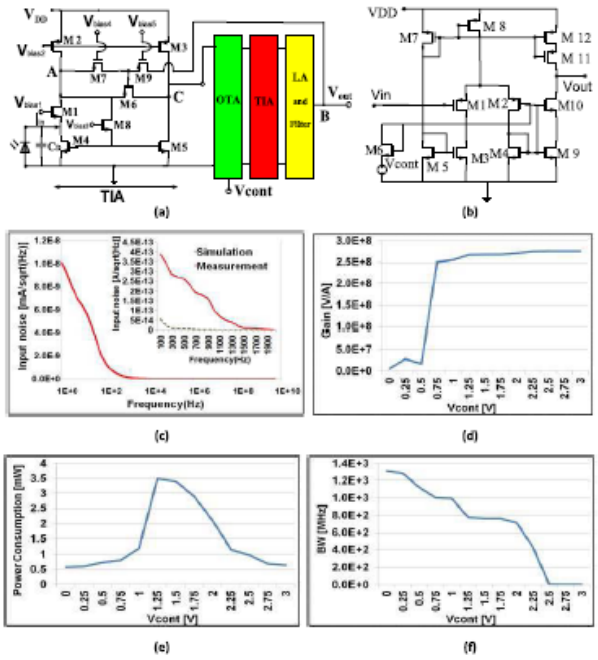

Fig. 5. (a) Schematic diagram of the proposed tunable TIA. M1, M6, M7, M9: W/L = 2.5/0.35, M8:W/L = 5/0.35 and for all other transistors W/L = 1/0.35. (b) Schematic of the OTA (M1, M2, M9, M10:W/L = 2/0.35, M11, M12: W/L = 10/0.35 and for all other transistors W/L = 1/0.35). (c) The input noise of the TIA front-end at different frequencies. The Gain (d), power-consumption (e) and BW (f) variation with different control voltages.

is possible to change the gain of the amplifier without varying the BW. We can use this fact in order to make the intensity of the photoreceptor independent to the BW variation and also increase the GBW of the circuit [29]. This is the technique applied in many organic photoreceptors [43], [44].

B. Proposed Tunable High-Gain TIA Front-End

The proposed TIA front-end, shown in Fig. 5(a), is formed by four stages. The first stage TIA provides a very low input resistance to handle the large photodiode capacitance (up to 5 pF) and the second TIA is also the same as the first TIA block. Using distributed gain concept in TIA front-end design increases the GBW of the circuit and allows changing the gain of the amplifier without varying the BW [29]. We have used this fact in order to make the intensity of the photoreceptor independent to the BW variation. In order to improve the differential input common-mode range (ICMR), DTMOS transistors have been applied. This proposed TIA structure is a combination of CG-TIA and RF-TIA topologies which we have already characterized it based

on the simulation at [28]. The design consists of a current amplifier implemented in a transimpedance configuration. In this circuit, we have used the combination of three transistors (M6, M7 and M9) biased in the linear region to act as a feedback resistor. Each transistor is comprised of three pairs of pass transistors as proposed in [39] in order to realize the desired gain-BW range. It offers the resitances with the

values of $R_{AB} = g_{mx}/2 = g_{m9}/2$ and $R_{AC} = 2g_{mx} = g_{m6}$ between node A and nodes B and C respectively. This minimize the output ripple and reduce the drained current. The dc transimpedance gain is given by:

$$\frac{V_{out}}{I_{in}} = -\frac{g_{M5}R_f - 1}{g_{M4} + g_{M5}} = -\frac{A_i R_f - R_{in}}{1 + A_i} \approx -R_f \approx 2.5g_{mx} \tag{8}$$

where g_{M4} and g_{M5} are the transconductance of transistors M4 and M5. The transimpedance gain is derived from the measured S-parameters of the TIA. Fig. 6(b) shows the comparison of the predicted transimpedance gain for the TIA obtained from calculated Equations. The gain and bandwidth predicted by Equation 8 are better than that of a TIA operating in a matching system which means the transimpedance gain will be overestimated using the calculated formula. Due to the rather slow signal variations in CW-fNIRS applications, usually a narrow BW is sufficient (1kHz for BOLD signal and 10–20kHz for neuronal signal). But offering a tunable high BW front-end will increase the performance of the overall system by increasing the speed for real-time monitoring in wireless device. The closed-loop BW of the TIA is approximately equal to the unity-gain frequency (the frequency where the loop gain of the TIA is unity):

$$BW \approx \frac{1 + A}{R_f C_D} \approx \frac{A}{R_f C_D} \approx \omega_t \tag{9}$$

CW-fNIRS applications measure rather slow signal changes (under 1kHz for BOLD signal and 10-20 kHz for neuronal signal), for this reason the importance of the bandwidth is relatively low but reaching high GBW value and robustness against power supply variations are very important. Here the GBW is equal to:

$$GBW = \frac{(g_{m1} + g_{s1})(1 - g_{m5}R_f)}{C_{in} + (g_{m1} + g_{s1})(C_L + C_f)R_f/K_{cm}}; \quad (K_{cm} = \frac{g_{m5}}{g_{m4}}) \tag{10}$$

where C_D, C_{in}, C_L and C_f are the photodiode, input, load and feedback capacitances respectively. BW of TIA increases by decreasing C_D.We have used C_D =1pF in simulations as this is the commonly reported value [21]–[23], [39]. In order to boost the voltage swing and match the output impedance to drive the photoreceiver output (usually a DMUX), we designed a Limiting Amplifier (LA) [29] and an OTA to be added to the output of the TIA. The OTA used in the proposed front-end amplifier design (Fig. 5(b)) is a current-mirror OTA, which is modified from the OTA reported in [5] and [28]. Performance of this OTA highly depends on the bias current and the sizing of the transistors. So we have considered these two parameters in order to reach the best performance. To increase the maximum output swing, and improve the stability of the circuit, we have also used a filtering block followed by TIA and LA. Because one of the main requirements of biosignal amplifiers is to have a wide dynamic range, here in order to achieve wide dynamic range, we have considered the proposed photoreceiver circuit as shown in Fig. 5(a) by adding the ability of parameters tuning. This is preferred

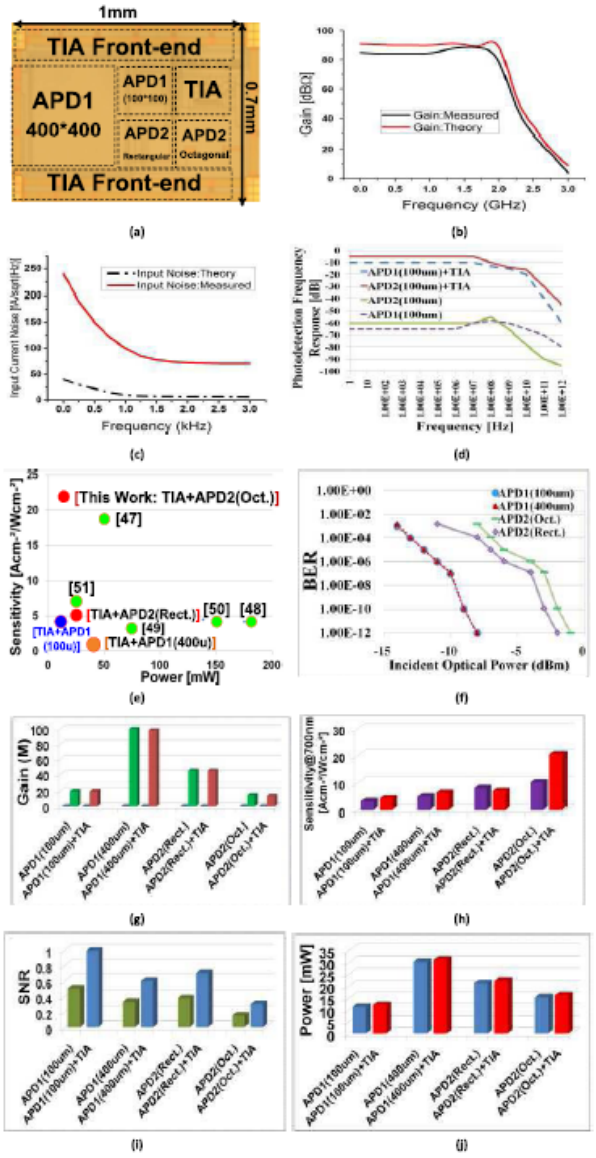

Fig. 6. The microphotograph of the fabricated IC (a), the transimpedance gain (b) and the input current noise density (c) of the integrated front-end at different frequencies. The Photodetection frequency responses of the CMOS integrated photo- receiver and CMOS-APD only (d) and Comparison of the Sensitivity/Power consumption of the proposed circuit with other works (e). The bit error rate (BER) as function of incident optical power when the input data has PRBS of $2^{31} - 1$(f). The impact of on-chip integration on different APD parameters: (g) Gain, (h) Sensitivity, (i) SNR, and (j) Power consumption.

to using output signal limiting and input current steering techniques to extend the dynamic range of amplifier. Using the constant applied voltage of $V_{cont}(0V < V_{cont} < 2V)$, the Gain, BW, power-consumption and dynamic range of the output could be changed in a wide output range (Figs. 5(d)-(f)). We need low-input noise for high-signal quality. Due to the low-frequency behavior of the signals, in-band noise of the readout is dominated by flicker (1/f) noise rather than thermal noise.

TABLE III

PERFORMANCE COMPARISON OF THE PROPOSED TIA WITH OTHER WORKS (C_P=1pF)

Ref.	Tech. (µm)		Supply voltage (V)	Power diss. (mW)	Max Gain	BW (MHz)	Input Noise at 1kHz (A/√Hz)	Max. Swing (V)	GBW/Power dis. (GHzΩ/mW)	Control
[5]	0.18		1	0.018	2.2 k	0.4	-	0.7	48.89	No
[17]	0.35		3.3	17	1.778k	1900	9.7 p	-	198.72	No
[28]	0.18		2	7.2	6.3 k	2500	<10 p	-	2187.5	Gain, BW
[36]	0.6		3	30	8.7 k	500	4.5p	-	145	No
[39]	0.35		1	1	210k	50	11 p	1	10500	No
[43]	0.18		2	19.5	12.6 k	2400	19 p	-	1550.77	No
[44]	0.35		3.3	53.5	501	2750	12.76 p	-	25.75	No
[45]	0.5		5	-	4 k	374	-	80m	-	No
This work: TIA	*sim*	*0.35*	*3*	3.15	200k	0.051	108 f	3	3.24	Gain, BW, Power
	mes	0.35	*3*	3.5	200k	0.051	112 f	3	2.91	Gain, BW, Power
This work: TIA+LA	*sim*	*0.35*	*2*	*1.5*	250 k	*11.9*	*41.7 p*	*2*	1983.3	Gain, BW, Power
	mes	0.35	*2*	*2*	250 k	*11.5*	*44.86 p*	*2*	1437.5	Gain, BW, Power
This work TIA+OTA+ TIA+LA	*sim*	*0.35*	*1*	*0.006*	90M	*0.013*	*19 f*	*1*	195 k	Gain, BW, Power
	mes	0.35	*1*	*0.010*	90M	*0.072*	*59 f*	*1*	6480 k	Gain, BW, Power
	sim	*0.35*	*3*	0.3	250M	1000	1 f	3	833.3 M	Gain, BW, Power
	mes	0.35	*3*	*0.8*	250M	*1000*	*100 f*	*3*	312.5 M	Gain, BW, Power

Combining the effects of all the independent noise components (ΣI^2_{flick}), the total input-referred noise current density of the TIA front-end can be calculated as [36], [39]:

$$I^2_{n,TIA} = \sqrt{\frac{4KT}{R_{in}}} + \sum \frac{K g_m^2}{WLC_{ox}^2}\frac{1}{f}\Delta f \approx \sum \frac{K g_m^2}{WLC_{ox}^2}\frac{1}{f}\Delta f \tag{11}$$

where k is Boltzmann's constant (1.38×10^{-23}JK^{-1}), T is the absolute temperature in Kelvin, W, L, and C_{OX}, are width, length, and the oxide capacitance channel of each transistor respectively. The equivalent input-noise current density (Fig. 5(c)) increases with the increase of capacitance of the APD. The noise measurements were done on bare chips by wafer probing. A low-noise preamplifier has been added before the noise figure analyzer to drive down the noise figure and decrease the measured noise figure uncertainty. Figure 6(c) shows the comparison of predicted equivalent input-noise current density for the proposed TIA by using the Equation 11 and the experiment. The equivalent input-noise current density predicted by Equation 11 is better than measured values, which means the equivalent input-noise current density will be underestimated using the calculated formula. The proposed TIA shows an ultra-low input noise characteristics (Fig. 5(c)). The TIA's equivalent input-noise current is reduced significantly using Current Balancing [14] and the noise cancelling [54] techniques. The noise

cancelling [55] used the fact that a virtual ground for the input-current is located at a point inside the feedback resistor. This node is used to cancel the noise of the TIA. By using the noise cancelling a high sensitivity optical receiver can be designed without increasing the power consumption. Noise cancelling is used for a low-noise amplifier (LNA) as applied in [56]. This allows for designing wide-band impedance matching amplifiers with small noise figure, without suffering from instability. Any noise source that can be modeled by a current source between the drain and source of the input device (e.g., 1/f noise, thermal noise of the distributed gate resistance, and the bias noise current injected into output node) is cancelled as well [54]. Referring to Table III, the input-current noise of the proposed TIA (Fig. 5 (c)) at 1 kHz is almost an order of magnitude better than other references using this technique. This also shows the efficiency of the applied topology and using DTMOS accompanyng with optimal transistor scaling based on the sensitivity analysis. Although there was a big discrepancy between the simulated and measured noises, the measured noise is extremely low comparing to all of the previously reported TIAs. The source of this difference is not completely clear, but the limited functionality of the applied spectrum analyzer and the capacitance variation due to the fabrication process can explain this discrepancy. In TIA the transistors M2-M1 forms a two-pole shunt negative-feedback loop that reduces the equivalent M2 source resistance. The input and output resistances of the TIA are calculated using:

$$R_{in} = \frac{v_{in}}{i_{in}} = \frac{g_{m5}}{g_{m4}+g_{m5}}(g_{m1}+g_{s1})^{-1} \;;$$
$$R_{out} = \frac{v_x}{i_x} = \frac{1+g_{m4}R_f}{g_{m4}+g_{m5}} \;. \tag{12}$$

We used CADENCE schematic editor and Virtuoso layout editor to design and simulate our proposed TIA in 0.35μm CMOS technology. This TIA front-end is fabricated using 0.35μm CMOS technology. The measurements were established on-wafer and using air-coplanar probes. The wafer probes were calibrated using the Line-Reflect-Match calibration method for S-parameter measurement [60], [61]. The complete four port S-parameters for the TIA were measured using on wafer probing with an HP8510 two-port vector network analyzer as [61]. Each of the measurements was taken over a frequency span of 1Hz to 5GHz with a total of 1000 points. The four port S-parameters were loaded into Agilent's ADS as a dataset and the circuit outputs were connected to an oscilloscope to see eye-diagrams as done by [60]. Using minimum length transistors we have aimed to increase the unity-gain current frequency (f_T) of the device by making the g_m, larger and the input capacitance, smaller and this can

TABLE IV

DESIGN SPECIFICATIONS OF THE PROPOSED INTEGRATED SiAPDs +TIA FRONT-END AND COMPARISON WITH DIFFERENT WORKS

Parameter \ Reference	[47]	[48]	[49]	[50]	[51]	[46], [52]	[68]	[67]	[66]	This work			
										TIA+APD1		TIA+APD2	
										Rectangular (100×100)	Rectangular (400×400)	Rectangular (100×100)	Octagonal (100×100)
CMOSTech.(μm)	0.18	0.18	0.13	0.18	0.13	BiCMOS 0.25	0.13	0.18	BiCMOS 0.25	0.35	0.35	0.35	0.35
Type	n-well/p-sub	SML	SML	Lateral PIN	P+/n-well	P+/n-well	P+/n-well	SMPD*	P+/n-well	P+/n-well	P+/n-well	P+/n-well	P+/n-well
Guard-Ring	n-well	n-well	-	n-well	p-well	p-well	STI**	-	STI**	n-tub	n-tub	p-well	p-well
Sensitivity(dBm)	-19	-4.2	-3.4	-4.5	-5.5	-3	-4	-6	-7	-4.3	-2.2	-6	-22
Data rate (Gb/s)	3	3.125	4.5	2.5	4.25	4.25	10	10	12.5	5.68	3.31	4.17	2.4
Log (BER)	-11	-12	-12	-12	-12	-12	-12	-11	-12	-13	-13	-12	-11
PRBS	$2^{31}-1$	$2^{31}-1$	$2^{7}-1$	$2^{31}-1$	$2^{31}-1$	$2^{31}-1$	$2^{7}-1$	$2^{7}-1$	$2^{31}-1$	$2^{31}-1$	$2^{31}-1$	$2^{31}-1$	$2^{31}-1$
Power (mW)	50	175	74.16	138	21.6	-	66.8	118	59	12	31	22	16

* spatially-modulated photo detector ** shallow-trench isolation

incorporate in a wide band design. However this may introduce somehow instability in gain and BW of the TIA due to the process parameters variation. In order to be sure this is not the case in our design, and in order to optimize the performance of the amplifier, using stability and sensitivity analysis the best values for optimal sizing were selected for the transistors to render the highest GBW while preserving the stability. The simulated and measured stability analysis shows a Phase margin of greater than 40°. The measurement results of the proposed circuit verify efficiency and reliability for a fNIRS system. Figs. 5(d-f) show the gain, the power consumption and the BW variation of the proposed circuit as a function of frequency and V_{cont}. For TIA: $Z_{in,dc} = 500\ k\Omega$, $V_{in,dc=0.5V}$, and for the total front-end: $Z_{in,dc} = 300\ \Omega$, $V_{in,dc} = 3\ mV$. By varying the V_{cont} in proposed variable-gain front-end (Fig. 5(a)), between 0–3V, we reached a very-high GBW value of 45×10^9. This value is tunable between 10M-45G for various applications.

We can reach the transimpedance gain in the range of 5-276 MV/A and BW in the range of 1kHz-1.31GHz using this configuration. The power consumption is in the range of 0.57-3.5 mW (Fig. 5(e)), making it suitable for medical wireless/portable applications. In order to verify the effect of the supply voltage, we have also tested the tunable-gain configuration by decreasing the supply voltage to 1V. The general specifications of the proposed TIA front-end are depicted in Table III. In order to validate the robustness of the circuit against power supply variation we have examined the TIA front-end characteristics for the supply voltages vary between 1-3.3V and the results for 1V and 3V supplies are measured. Here the M1-M2 and M7-M9 have been biased independently at 1-3V power supply operation to insure their functionality. Thanks to using complementary body driving technique [69], [70] and DTMOS transistors, the circuit functionality was guaranteed in 1-3 V bias variation. As the results are shown for three different points (1V, 2V and 3V) in table III, the performance does not degrade significantly despite power supply variation. In 1V bias voltage the front-end circuit shows better characteristics regarding to power and input referred current noise. However, low-bias operation implies maintaining the bias of M1-M2 and also M7-M9 transistors independently in different bias values. Furthermore, the low-bias condition imposed a drastic phase-margin degradation and output instability, so it is not recommended without using extra compensation circuitry [39], [71].

A large discrepancy is observed between simulation and measurement results of the power consumption and the input-noise as shown in Table III. By considering the ultra low-level of the measured noise and power, the cause of this different is most likely a combination of effects. This can be due to the effects of the used bonding pad parasitic capacitance or the limited accuracy of the test setup used to get these values. There could be coupling between the measurement probes, as well as effects from the rest of the measurement setup. The final layout of the designed integrated circuit after post-layout simulation and optimization was fabricated by TSMC 0.35 μm via CMC. This 18-pin IC has the die size of 1.5mm×2mm, and includes proposed APDs and the amplifier. The microphotograph of the fabricated IC is depicted in Figure 6(a). The fabricated test chip includes several APDs, TIAs and also the integration of APD+TIAs in order to verify the functionality of different configurations and effects of integration. Here in this paper we have reported the detailed measurements after a systematic study over more than 20 different chips. Several packages and wire-bonds were also made to have access to the different components. The reported values here show the average value of the results for functional circuits. The observed measured variances for each parameter are also shown in this table. To analyze the variation of measured parameters between different chips, the variances of different parameters of all APDs for evaluated chips are measured. The observed fluctuations in APD1 (APD2) include: The device-device fluctuation for =±1.01V (±1.5V), PDP=±13% (±18%), Dark current=±15nA (±21nA). The wafer-wafer fluctuation for V_{br}= ±0.7V (±0.7V), PDP=±9% (±9%), Dark current=±0.5nA (±0.5nA). The chip-chip fluctuation for V_{br}=±0.9V (±1V), PDP=±11% (±15%), Dark current=±2.5nA (±3.3nA).

The final measurement results of the proposed TIA front-end are compared with results from the literature in Table III. This design has the highest transimpedance gain and the lowest power consumption and input/output noises accompanying with a suitable gained performance regarding to the on-chip integration of APD and TIA.

IV. APD+TIA Integration

To increase the use of photodetector systems for state-of-the-art biomedical applications, integration of the SiAPD and the high-speed peripheral circuitry on the same chip using standard CMOS technology is highly desired. Here the proposed SiAPDs and TIA front-ends have been integrated on the same chip and the measurement results regarding to this integration are shown in Table IV. For the wavelength-specific applications also the spectral sensitivity of the detector should be considered. The bit error rate (BER) as function of incident optical power is depicted in Figure 6 (f) for different APDs. The gain, sensitivity, SNR, and power consumption for each CMOS-APD separately and for the integrated photoreceiver (APD+TIA) are measured and compared in Figs. 6 (g)-(j) in a normalized scale. In order to verify the impact of the applied APD structure and scale on these different measured values, this comparison has been established for different APDs. Referring to these comparison plots, and regardless of the applied APD structure we see a regular variation in each examined parameter. A significant improvement in sensitivity, SNR, noise and size are gained in integrated circuit with the cost of higher-power consumption. No significant change was observed regarding to the multiplication gain and BW. Furthermore these results show that the impact of integration is mainly on SNR and then on the power, sensitivity and noise respectively. In addition to the photon detection efficiency and dark count rate that limit the minimum detectable power, the dynamic range (DR) which is define as the ratio between the maximum and minimum detectable power is also an important parameter that is 80dB and 92dB for APD1 and APD2 respectively. A similar trend is observed regarding to the SNR, noise, gain and power variation in all 4 APDs, except for sensitivity. This can be due to the high dependency of the APDs sensitivity to the input impedance and BW of the applied TIA in contrast to the other parameters. In Fig. 6(d) the Photodetection frequency responses (PFR) of the CMOS integrated photoreceiver and the independent CMOS-APDs when $Vr = 9$ V and incident optical power $= 0$ dBm are compared. While the PFR for the proposed APDs is not high, the integration improves the PFR significantly. As the reverse bias voltage is increased, the photodetection frequency response increases because of increased avalanche gain. Optimization of the CMOS-APD using rf-peaking [51] can enhance photodetection 3-dB bandwidth while maintaining sufficient avalanche gain. The maximum 3-dB bandwidths for the integrated circuit of APD1+TIA and APD2+TIA are about 3.79 GHz and 2.78 GHz at the reverse bias voltage of 10.6 V. Integrated circuit specially regarding to the square APD2 offers better bandwidth performance compare to APD1. The characteristics of the proposed circuit are shown comparing to the other works in Table IV. In addition, the Fig. 6(e) also depicts more clearly the power and sensitivity preference of the proposed integrated circuit comparing to other works.

V. Conclusion

In order to overcome the limitations of currently available non-portable fNIRS systems, a new miniaturized, reconfigurable and low-noise light detector has been introduced in this paper. It includes a new TIA integrated with two new SiAPDs on the same chip using CMOS 0.35μm technology. Proposed rectangular and octagonal SiAPDs offer the avalanche gain of 100 and 45 with the breakdown voltage of 6V and 9V and the photon detection efficiency of 45% and 25% at 800nm respectively. Fabricated TIA front-end has high transimpedance gain (up to 250MV/A), tunable BW (1kHz-1GHz), extremely low input and output noise (100fA/$\sqrt{}$Hz, 1.8μV/$\sqrt{}$Hz), high stability (phase margin$\geq$40°), robust against power supply variations and low-power consumption (0.8mW), all the essential requirements for fNIRS photoreceiver front-end. The proposed TIA front-end also shows efficient results in two different bias voltages. The on-chip integrated APDs with the proposed TIA preserves the high-performance characteristics of both APDs and TIA while offering a more compact photodetector front-end with high fill factor to be used in arrays of detectors in different optical detectors and for low-intensity light detection applications.

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APPENDIX 4 – PAPER #3

A Low-Power Photon-Counter Front-End Dedicated to Neurovascular Brain Imaging

A Low-Power Photon-Counter Front-End Dedicated to Neurovascular Brain Imaging

Ehsan Kamrani, *Member IEEE*, Frederic Lesage, and Mohamad Sawan, *Fellow IEEE*

Abstract— **This paper introduces a new miniaturized on-chip photodetector front-end to be applied in a portable near infra-red spectroscopy (NIRS) system as a non-invasive tool for real-time neurovascular brain imaging. It includes silicon avalanche photodiodes (SiAPDs), a Transimpedance amplifier (TIA) with on-chip gain/bias control, a new controllable mixed (active-passive) quench circuit, with tunable hold-off time, and a novel Gated Quench-Reset technique. Implemented SiAPDs exhibit avalanche gain of 35 and 22 at 10V and 18V bias voltages with peak photon-detection efficiency in near infra-red light spectrum and dark count-rates of 114kHz and 4kHz (at 1V excess bias voltage). The implemented TIA consumes 1mW power, and offers a transimpedance gain of 250 MV/A, a tunable bandwidth (1kHz-1GHz), and an input current referred noise less than 10fA/√Hz at 1kHz. The implemented photon-counter exhibits a quench-time of 10ns with a 0.4mW power-consumption accompanied with more flexibility and high-dynamic range of operation by developing an adaptive hold-off time control. This integrated photoreceiver front-end has been implemented using submicron standard CMOS technologies with a minimum fill-factor of 95%. The on-chip integration of SiAPDs and front-end circuitries, has reduced the power-consumption and after-pulsing, and increased the sensitivity.**

Index Terms—**Avalanche Photodiode, Biomedical Imaging, High-speed Photon-Counting, Low-power Integrated Circuit.**

I. Introduction

SINGLE-PHOTON avalanche photodiodes (SPAD) operating in Geiger-mode, due to their internal gain characteristics, have shown potential for high-sensitivity and low-intensity light detection applications. An infinite self-sustaining avalanche current flows through the SPAD with impact of a single photon into its surface which can be counted as a pulse at the SPAD output. The duration of the avalanche current produced by incident photon in SPAD must be as short as possible to avoid excessive power-dissipation and device destruction. In order to operate the SPAD for single-photon counting, a Quench-circuit has to be used to suppress and quench the avalanche current, and a Reset-circuit is also required to reset the SPAD bias to its initial condition after a hold-off time and prepare it for subsequent avalanche and counting the next photons.

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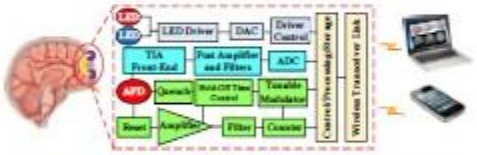


Fig. 1. Block diagram of the introduced NIRS brain imaging system.

Available SPAD control and processing modules are typically implemented using FPGA [1],[2] capable of controlling a single parameter with a limited speed. The traditional control systems for photodetection are based on automatic gain, bias or temperature control. These control blocks are off-chip and/or have been designed in order to control over a limited range of temperature or gain variations and require additional circuitry for providing thermal stabilization for SPAD to avoid full breakdown of avalanche photodiodes (APDs). In traditional time-correlated single photon counting (TCSPC) detectors [20] applied in tomography, using digital circuitry imposes more complexity, higher power-consumption, lower-speed and higher-cost. The variable and uncontrollable gain of the APD can take it into full avalanche breakdown which can cause catastrophic and irreversible damage to the APD itself. The noise from the APD is also an increasing function of gain so it is desirable to operate the APD such that the gain is just sufficient to bring the shot noise amplified by the avalanche process to the level of the thermal noise of the preamplifier. Furthermore, the background level variation, changes the optimum value of the gain. So maintaining an optimum gain and bias for operating the APD is a critical challenge in designing a photodetection system based on APD.

The high power-dissipation due to the slow avalanche current can drift the breakdown-voltage, and change the SPAD response regarding to the detection efficiency and noise. Delayed release of trapped-charges due to the large charge trapping in SPAD can retrigger the detector and cause false ignitions (after-pulsing). After-pulsing cause a non-linear distortion in photon-counting [8]. Decreasing the avalanche time duration reduces the power-dissipation, charge-trapping and the optical crosstalk due to the minimization of the hot-carrier photon-emission [8]. The main available quench-reset techniques include: passive (PQC) [9], active (AQC) [10], and mixed quenching (MQC) [11]. Here we have designed and implemented a miniaturized photon-counting system including a high-speed and low-power photon-counting circuit integrated with silicon CMOS avalanche photodiode (SiAPD).

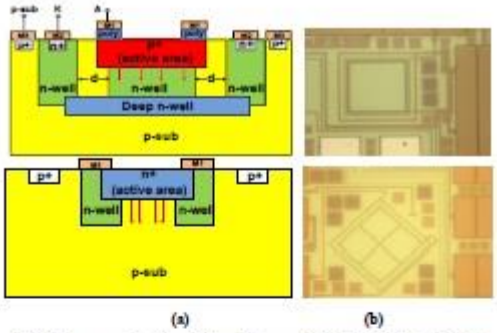


Fig. 2. Cross-section (a), and microphotograph (b) of the fabricated APD1 (first row), and APD2 (second row).

Table 1. Characteristics of the implemented SiAPDs

Parameters	APD1	APD2
CMOS Technology	0.18 µm	0.18 µm
Multiplication Gain	35±10 (@Vbias=10V)	22±10(@Vbias=18V)
Breakdown Voltage	12±3 V	19±2 V
Dark Count-Rate	114±1kHz(@Vex=1V)	4±1kHz(@Vex=1V)
PDE* (@700nm)	15±3%	39±7%
Impedance	0.8 ± 0.18 Ω	20.3 ± 0.07 Ω
Capacitance	1.3±0.1 pF	0.41±0.02 pF
Noise-Factor:F (@M=20)	61±0.1	39±0.14

*Photon detection efficiency

This Geiger-mode or single-photon avalanche diode (GM-APD) device may allow low-intensity light detection in medical imaging applications such as brain imaging using TCSPC and computed tomography (CT-Scan). The implemented circuit in this work is going to be applied in a portable near infra-red spectroscopy (NIRS) system as shown in Fig. 1. The on-chip integration of the SiAPD and TIA and the wireless link has been already introduced in [3], [4], [5]. This paper reports the realization of an on-chip integrated controllable photon-counter using standard CMOS technology. In the following, the implemented low-voltage NIR SiAPDs and the amplifier front-end are introduced in section II. Then the implemented photon-counter front-ends for passive, active, mixed and controllable-mixed quench (CMQ) are introduced in section III and IV followed by the experimental results and discussions on introduced CMQ in section V.

II. Implemented SiAPDs and Amplifier Front-End

A. SiAPDs

A Rectangular-shape p+/n-well with an active-area = 100µm×100µm and a p-sub guard-ring is implemented using standard CMOS process (APD1). Its cross-section and microphotograph are shown in Fig. 2(first row). In order to confine the avalanche process under the active area in APD1, a deep n-well layer is implemented under active area between n-well and p-sub as shown in APD1 structure.

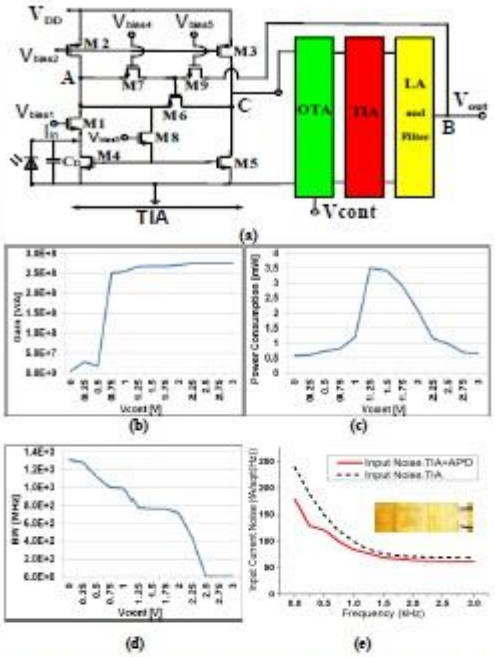


Fig. 3: (a) Circuit of the implemented tunable TIA. The Gain (b), power-consumption (c) and BW (d) variation with different control voltages. The input noise of the individual and integrated TIA at different frequencies (e).

An n+/p-sub SiAPD (APD2) has also been implemented in quadratic topology shown in Fig. 2 (second row). APD2 is a Quad-Rectangular net n+/p-sub SiAPD with active area of 100µm×100µm. The specifications of these SiAPDs are summarized in Table 1.

B. TIA Front-End

The implemented four-stage Transimpedance amplifier (TIA) front-end is shown in Fig. 3(a). The core TIA is based on the combination of a sub 1-V current mirror and a common-gate current-gain amplifier. In order to improve the differential input common-mode range (ICMR), dynamic threshold metal-oxide-semiconductor (DTMOS) transistors were used in a combined common-gate and resistive-feedback topology. The main characteristics of this TIA are shown in Table 2. This distributed-gain TIA offered a lower-noise (×0.001), higher GBW (×25) compared to the single-stage TIA, while provided a tunable power, gain, and BW (Figs. 3(b)-(d)) and high-stability (phase-margin≥40°). It offers a maximum transimpedance-gain of 250MV/A, a tunable-BW in 1kHz-1GHz range, the input and output noises of 100fA/√Hz, and 1.8µV/√Hz respectively, and a maximum power-consumption of 0.8mW. The in-chip integration of this TIA with APD has improved its efficiency especially regarding to the noise and SNR characteristics (Figure 3(e)).

Table 2. Characteristics of the implemented TIA Front-End

Parameters	TIA	TIA+AGC
CMOS Tech.	0.35 µm	0.18 µm
Gain (MA/V)	250	298
BW (Hz)	100Hz-1GHz	10Hz-5 GHz
Input Noise	100 fA/√Hz	10 fA/√Hz
Power Consumption	0.8 mW	0.5 mW
Bias Voltage (V)	3	1.8

III. GEIGER MODE CIRCUITRY DESIGN

A. *Passive and Active Quenching Circuits*

The schematic of the implemented PQCs are shown in Fig. 4(a)-(b) in two possible voltage and current mode configurations. The voltage-mode PQC provides longer pulses, which might be convenient to visualize them in the oscilloscope but might hinder high-speed detection and the detector timing performance is not fully exploited. On the other hand, the current-mode output PQ configuration allows high detection-rates [11], [12]. Here R_L is the load resistor (typically between 50KΩ and 500KΩ) and R_S provides matched termination for a coaxial cable (~50Ω). When no current flows in the circuit, the SPAD is reversed biased at Vop. When a photon arrives a photo-generated current flows through the SPAD. As shown in Fig. 4 (c)-(d), the photo-current flows through R_L at this time and it causes the voltage in SPAD cathode and therefore its bias voltage reduce and suppresses the avalanche current. The large time-constant of PQ circuit prevents the bias voltage from dropping rapidly.

This results in an avalanche quenching delay and hence inaccuracy in the photon-arrival detection and increases the power-consumption and consequently the SPAD temperature. However the PQC is a simple quenching technique, but it suffers from low-speed, high power-dissipation, limited maximum operation frequency (< few hundred kHz) and it is usually bulky due to its high value resistor (R_L). PQ is suitable for APDs having small area and small RC time contacts since it can be operated at higher speed. They can also be used with large-area devices where high counting-rates are not a requirement. In order to achieve faster quenching, AQC is used. This method forces back on the SPAD to drop the bias voltage much quicker enabling significant speed improvements over the PQ method. This technique offers high-accuracy, lower after-pulsing and lower-power consumption (hence less heating of the SPAD). Dead-time of the circuit does not depend on the component values and can be accurately controlled; hence determination of precise dead-time is possible for satisfactory circuit operation. However, these advantages achieved with the expense of stringent circuit requirements. It is difficult to design an effective AQ circuit and it needs complicated precise circuitry to reduce the propagation-delays as well as the stray-capacitances.

B. *Mixed Quenching Circuit (MQC)*

Here the previously applied active and passive techniques are combined to form a hybrid approach [13], [14]. In MQC, the passive - quenching is used as the first stage to limit the avalanche current to a low-value, followed by the application of a quench pulse during the quench delay time and a reset pulse to recharge the SPAD back to the reverse bias voltage higher than Vbr. In this method a current-mode PQ circuit is applied at the first stage which increases the detection-rate comparing to the voltage-mode PQ circuit with longer pulses. The incident light intensity information is obtained by counting the pulses during a certain time frame or by measuring the average time interval between successive pulses. Due to the complementary action of the active quench circuit in MQC in order to repress more the initially quenched avalanche by PQC, there is more flexibility in choosing the PQ load (R_L). Therefore by reducing R_L one can achieve a quicker detection of the photon [15]. By increasing the light intensity received by the APD, the current flow through the diode and R_L will also increase. The resulting increase voltage drop across R_L, decreases the bias voltage across the APD, so that the gain of the APD is reduced. Therefore the dynamic-range of the optical input of the APD will be increased for a fixed dynamic-range of electrical output. Using this circuit, faster quenching results in lower power-loss and hence less heating of the SPAD [16].

The schematic of the implemented mixed Quench-Reset circuit is shown in Fig. 5(a) [17]. In this circuit, the transistor M1 is biased in common-source mode with M3 as an active nMOS load. The transistor M4 is used as diode to provide the self-adjusting bias to the load M3 (the same for M2 and M6 which provide the self-adjusting bias to M_{Reset} and M5 respectively). Here the M_{Quench} and M_{Reset} are the main transistors for Quenching and Resetting the APD. The transistor M_{Select} is ON by default but it can be used to torn ON/OFF the Quench/Reset process or in APD arrays to select a specific row of photodetectors.

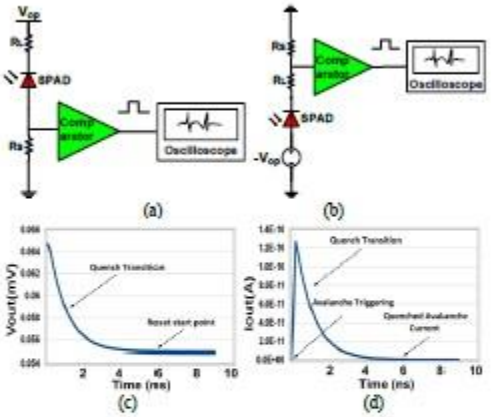


Fig. 4: Schematic of the passive quench circuit in two possible voltage and current mode configurations (a)-(b). The APD cathode voltage (e) and current (f) in response to single photon arrival with Vop = 20 V, RL = 200 kΩ, and Rs = 50 Ω.

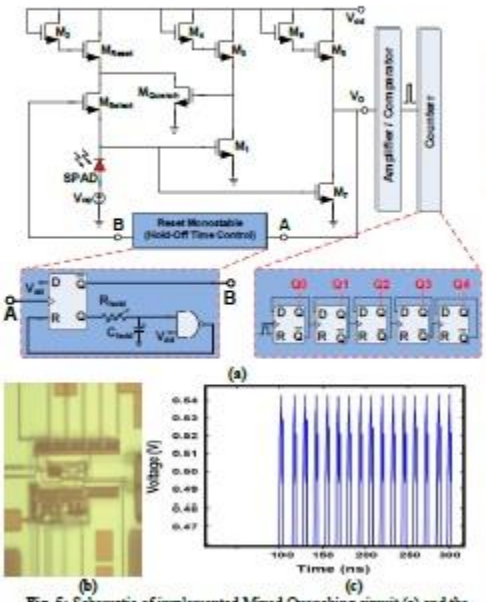


Fig. 5: Schematic of implemented Mixed Quenching circuit (a) and the microphotographs of the fabricated IC (b). The main transistors scales are as: M2=220nm, M3=95µm, M4=16µm, M5=21µm. The Oscilloscope screen capture quenched APD Output (c).

This transistor (M_{Select}) connects the transistor M_{Reset} to APD cathode and charging the APD to the V_{BR}. By incident of the photon, the avalanche is initiated. This cause an voltage drop across APD. The M1 transistor amplifies the signal with a phase-shift. The amplified output of the M1, turns on the M_{Quench} transistor which pulls down the APD bias voltage bellow the V_{BR}. This quenches the APD output and the avalanche process would be completed. The Quench and Hold-off times can be controlled using Control-block connected to the M_{Select}. If the M_{Select} be activated by control block after a controllable hold-off time, then the M_{Reset} transistor, resets the APD by biasing it over its breakdown voltage. The generated pulse from the digitizer is detected by the D-flip flop, which is rising-edge sensitive. The APD cathode voltage is maintained constant during the hold-off period and then an enable pulse is generated. It discharges the APD back to its genuine operation level by activating low-resistance M_{Select} for detecting the next photon. The hold-off time is chosen with respect to the $R_{hold} \times C_{hold}$ value. The enable pulse for activating M_{Select} is generated through a NAND gate, followed by an inverter. The reset process should be as fast as possible to avoid dark-current noise. The reset-time for the designed circuit is 1-4ns. The choice of hold-off time is an application-dependent issue. In fact, there is a unique choice for the given application which might be affected by the nature, density and lifetime of the generated traps in specific APD.

Table 3: General Characteristics of the implemented Mixed Quench Circuit

Parameter	Simulation	Measurement
CMOS Technology	0.18 µm	0.18 µm
Layout Size	50µmx120µm	50µmx120µm
Power consumption	2.14mW	1.70mW
Input Impedance	2 Ω	2.8 Ω
Output Impedance	1.58 kΩ	1.24 kΩ
Quench Time	3ns	100-200 ns
Dead-Time	7ns	7 ns

The hold-off time should be long enough to allow trapped carriers to be emitted and minimizes the after-pulsing which may affect the photon-counting statistics. On the other hand, hold-off time should not be too long to avoid limiting the repetition rate which may intervene the system settling time fetching new photon detection procedure. Considering the application requirements, the hold-off time is in the range of 4ns-2µs which could be set by tuning the value of C-Hold and R-Hold [17], [18].

The measured output response to multiple-photons is shown in Fig. 5(c) and the main characteristics of the circuit are summarized in Table 1. The high discrepancy observed between simulated and measured quench-time may be due to the unspecified resistance and capacitances imposed by the pad, wire-bonding and the measurement setup. The implemented MQC method adopts a simpler design while still allowing some control over the dead-time and the use of a voltage pulse to speed up quenching. The value of the load resistor that provides the initial passive quenching action is lower as compared to pure PQ since the actual quenching is done by AQC block [13]. However, the switching delays related to the relatively large parasitic capacitances and relatively high-value PQ resistance of the circuit limit the performance and quenching speed of the MQC [15], [19] and it needs more circuitry and extra size [16].

IV. Implemented Controllable MQC

Here we have developed a new quench-reset technique called Controllable mixed-quench circuit (CMQC), shown in Fig. 6(a). Its quench part is based on the introduced MQC technique in [13], and it has been modified to offer a higher-speed, lower-power and lower-complexity accompanied with more flexibility and dynamic range of operation by developing an adaptive and faster hold-off time control on the previously implemented MQC. We have used a current-mode PQC at the first stage which increases the detection rate comparing to the voltage-mode PQC circuit with longer pulses applied in [13].

In quiescence condition, the cathode of SPAD is biased to V_{dd} (usually 5-10% above the breakdown voltage for achieving higher sensitivity) through R1 and is ready to detect a photon. The onset of the avalanche current starts a passive quenching action and the voltage drop across R1 reduces the voltage at the SPAD cathode. As such, S_{sense} goes in deeper conduction and the voltage drop caused by R3, turns the quench transistors ($S_{quench1}$ and $S_{quench2}$) ON via $S_{feedback}$.

This starts the active quenching action by quickly pulling the SPADs cathode down to ground. This brings the reverse bias of the SPAD below breakdown and the avalanche current quickly dissipates. The quench transistors ($S_{quench1}$ and $S_{quench2}$) are then turned OFF and the three parallel reset transistors (S_{reset1}, S_{reset2}, and S_{reset3}) are turned ON.

The reset transistors are activated by an output pulse from the reset monostable which triggers with the end of the hold-off period. These reset transistors are equivalent of the three low resistance transistors, which resets the quiescent bias of the SPAD and brings the SPAD cathode voltage back to detect the next photon. Short duration of the reset-time decreases the dead-time between photon counts. The dead-time of the circuit (Quench+Reset time) does not depend on the component values and can be accurately controlled to be matched with desired circuit operation using a timing circuit (Fig. 6(b)) [21]. Using implemented CMQC, reduces the required size of load resistor (R_L) and so the power-consumption, charge-trapping, after-pulsing and the optical crosstalk and also improve the performance by quicker detection of the photon in a wider dynamic-range optical input. This circuit improves the SPAD performance which is directly proportional to the amount of the excess electric bias voltage above the breakdown voltage (V_E) given by:

$$V_E = V_{dd} + |V_{op}| - V_{BR} \quad (1)$$

where the bias voltage is provided by circuit supply voltage (V_{dd}) and a DC voltage (V_{op}) connected to the APD anode. Using this circuit, results in a faster quenching with lower power-loss and hence less heating of the SPAD.

A Gated photon-counter (GPC) depicted in Figure 6(b) is used to record the intensity of a high-repetition rate pulsed signals in a fixed time window defined by the gate-pulse triggered externally by SPAD. It includes a discriminator that has an adjustable threshold, which is set to discriminate the single-photon pulses against the background noise. In this system, the APD is biased just below the breakdown voltage and a gated-pulse (Figure 6(c)) is used to drive it above breakdown for a short duration. An incoming photon during this gated pulse triggers the avalanche leading to a large current. By exceeding from the threshold, the discriminator produces a pulse with a specific level and duration (Fig. 6(c)). The GPC improves the time resolution, baseline stability, and SNR, by suppressing the background counts from the detector in the time intervals where no signal is presented [22].

However, its efficiency is low because of the rejection a large part of the detected photons by a narrow gate. In order to improve the efficiency of the GPC, here we have implemented a multiple-gate photon counting (MGPC) architecture shown in Fig. 6(d). In this method the detector photon pulses counted directly using several parallel gated counters. The gates are controlled using separate gate delays and by separate gate pulse generators to yield a counting efficiency close to one.

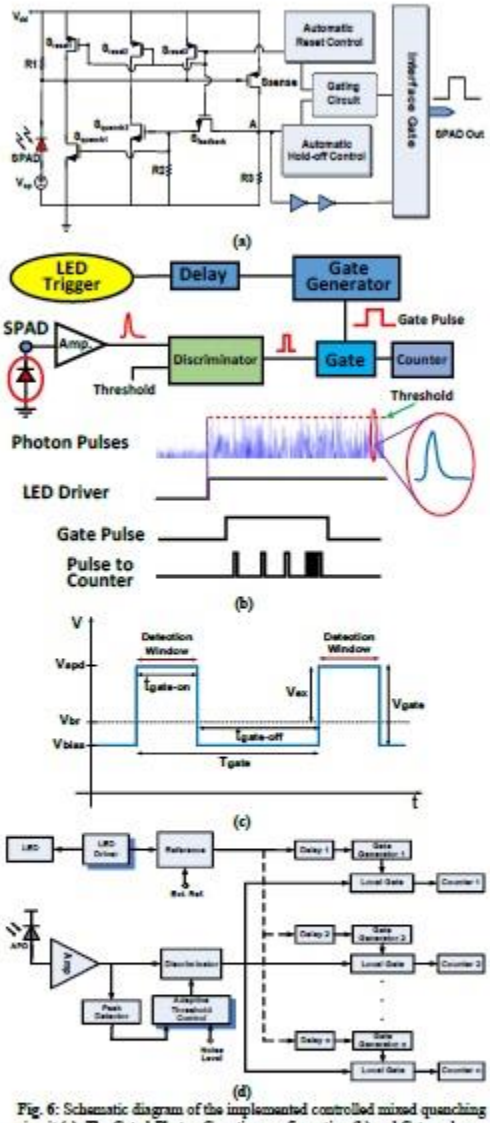


Fig. 6: Schematic diagram of the implemented controlled mixed quenching circuit (a). The Gated-Photon Counting configuration (b) and Gate-pulse details (c). The implemented multiple-gate photon counting architecture (d).

The threshold in discriminator has been set well above the noise-level, but below the peak amplitude of the detector photon-pulses. An adaptive-threshold control block introduced in [23] and [24] is implemented for real-time threshold allocation based on the noise background, the system noise-level, and the amplitude of the APD pulses.

V. Results and Discussion

A. Experimental Set-Up

The introduced CMQC system is implemented and fabricated using standard CMOS 0.18 µm technology (Figure 7(a)). In order to characterize the fabricated CMQC photon-counter, we have developed an experimental setup as shown in Fig. 7(b). For wafer-based measurements, the test setup secured the wafer to the probe station platform via vacuum and used probes to contact the metal pads for measurement devices. A dark cover was used to block any stray light, which would affect the measurements, and all light sources in the room were turned off. The background light-leakage was measured using a calibrated large-area photodiode (Hamamatsu S9295-01). The number of incident photons per second on the device was calculated using measured output voltage and gain of the APD for the room light (as established in [27]).

Figure 7(c) shows the outputs of the implemented CMQ circuit in response to the single and multiple photon arrivals and the main characteristics of the introduced techniques are summarized in Table 4. Using CMQC circuit, faster quenching resulted in lower-power loss and hence less-heating of the SPAD. The SPAD Response-speed (rise-time) is defined using cutoff frequency determined by the RC time constant as: $t_r = 0.35/f_{c,RC}$ where $f_{c,RC} = 1/2\pi C_t R_L$. The rise-time of the output signal is a few fs. The decay-time depends on the recovery-time thus on the quenching-circuit, which for the PQ the time constant given by the RC product. Both the rise-time and decay-time increase with the total capacitance of the APD. The APD capacitance increases with its area with typical values being 1.3pF for APD1 and 0.41pF for APD2. The measured power-consumption of the fabricated chip is 0.4mW. It exhibits a controllable hold-off (in the range of 1ns to 5µs) and rest time (with minimum value of 6ns) and a short quench-time of 3ns.

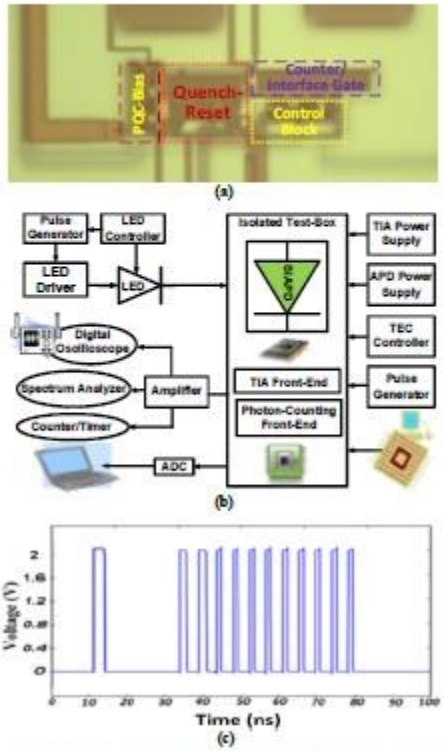


Fig. 7: The microphotograph of the fabricated circuit (a). The general applied measurement set-up (b) and the APD cathode voltage in response to single photon (at 10ns) and multiple-photon arrivals between 35ns-80ns (c).

B. Gain Characteristics

The accurate measurement of the APD multiplication gain (M) is a critical requirement for APDs due to the high background and detector noise. It is calculated using following formula:

$$M = 1/(1 - \int_0^L \alpha(x)dx) = 1/(1 - (\frac{V}{V_{br}})^n) \quad (2)$$

where L is the space charge boundary for electrons and α is the multiplication coefficient for electrons (and holes), strongly dependent on the applied electric field strength, temperature, and doping profile. n ($2<n<6$) is a constant depending on the semiconductor used for the construction of the transistor and doping profile of the collector-base junction. The applied gain measurement set-up is shown in Fig. 8(a). The APD is lighted with a stable, continuous, light source and the current flowing trough it is measures as a function of the bias voltage (I_{on}).The same measure is repeated turning off the LED (I_{off}).

The Gain then is calculated by:

$$G(V) = \frac{I_{on}(V) - I_{off}(V)}{I_{on}(G=1) - I_{off}(G=1)} \quad (3)$$

The multiplication gain depends on the bias voltage and it can also be measured by calculating the ratio between the photo-current of the tested detector and that of the calibrated one. In order to measure the APD multiplication gain, the APD outputs are plotted before the breakdown. The multiplication gain then is measured as absolute ratio of the voltage amplitudes in these two signals. Figures 8(b)-(c) show the measured gains of the implemented APD1 and APD2. The measured multiplication gains at different excess-bias voltages for different temperatures are shown in Figure 9 (d).

Uncertainties on the gain measurement directly affect the photon detection efficiency (PDE) values. The Gain uniformity between CMOS APDs fabricated on the same die and on different dies in the same production batch is shown in Figure 8(e).

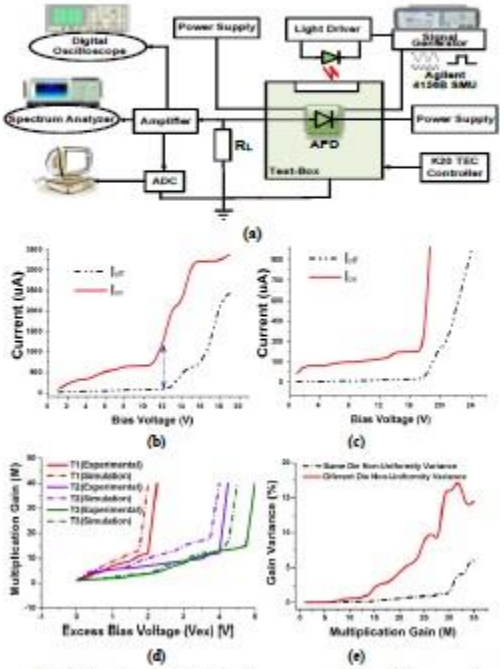


Fig. 8: Experimental setup for gain measurement (a), and the measured dark-current and photo-current of APD1 (b) and APD2 (c) for gain determination. The M-V plot in different temperatures where $T_1 = -25^{\circ}C, T_2 = -25^{\circ}C, T_3 = -25^{\circ}C$ (d), the Gain uniformity between CMOS APDs fabricated on the same die and on different dies in the same production batch (e)

C. PDE Characteristics

The electro-optical setup for PDE measurement is shown in Fig. 9(a). The PDE has been measured using two different techniques explained here:

(a) The Photo-current method: In this case the setup shown in Fig. 9(a) is simplified by substituting the amplifier, the discriminator and the counter with an Ammeter. Two photodiodes have been used, one as reference detector, the other is the detector to be tested and the measurements have been done of the photo-generated current in both sensors. The photo-current of the detector is then measured with respect to the calibrated reference APD. The Photodiode and detector under test have been chosen to be close together to guarantee equal luminosity [29], [28]. The PDE is then has been calculated as follow:

$$PDE = \left(\frac{I_{on}-I_{off}}{I_{on1}-I_{off1}}\right) \times \frac{1}{M} \times PDE_1 \times \frac{A_1}{A} \qquad (4)$$

where I_{on} (I_{on1}), I_{off} (I_{off1}) and A (A_1), are the photocurrent, dark current, and active area of the under test SPAD (and reference SPAD), respectively. The M and PDE_1 indicate the Gain and PDE of the reference SPAD.

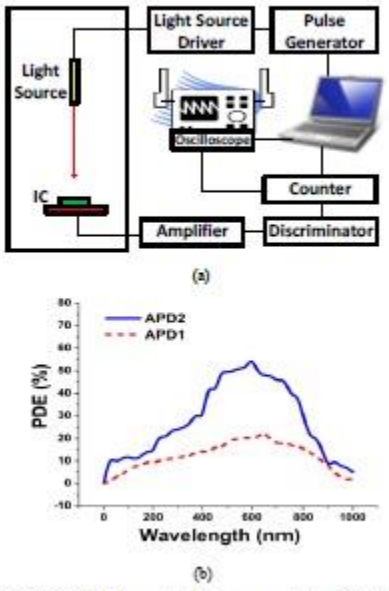
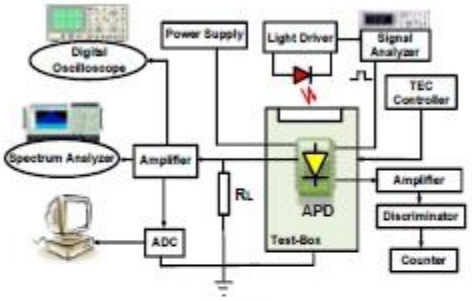


Fig. 9: (a) Block diagram of PDE measurement setup. (b) The PDE characteristics of the APD1 and APD2.

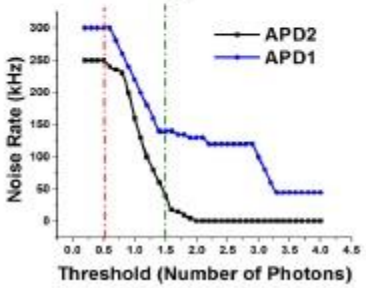
(b) The Photon-counting method: It is based on measuring the SPAD count-rate (CR) due to the real photo-events and comparing it to the photocurrent measured by the Ammeter converted into number of electrons per second. The PDE is then calculated as follow:

$$PDE = \left(\frac{CR_{on}-CR_{off}}{I_{on1}-I_{off1}}\right) \times \frac{1}{e} \times PDE_1 \times \frac{A_1}{A} \qquad (5)$$

Comparison of the results from these two techniques showed a significant PDE overestimation in the photo-current method compare to the photon-counting technique. We demonstrated unequivocally that this is essentially due to the fact that the photocurrent technique cannot discriminate the after-pulse and the cross-talk effects. On the contrary, the photon counting method allows to characterize and accurately discriminate the two noise effects providing PDE values quite close to the real ones, but needs to operate in appropriate signal conditions, in fact very fast events can be lost and the total counted events can be lower than those expected. Then we can conclude that the photon counting is a method well suited for PDE measurements because it definitely deals with true photons, reducing as much as possible the contribution of extra pulses. In order to obtain accurate measurements in photon-counting technique, we have adjusted the photon flux-level in such a way that the reference detector was still sensitive and the detectors were safely in the single-photon regime with negligible pile-up (a similar technique is applied by [28]). Figure 9(b) shows the measured PDE for APD1 and APD2.

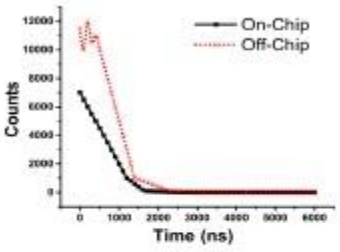


(a)

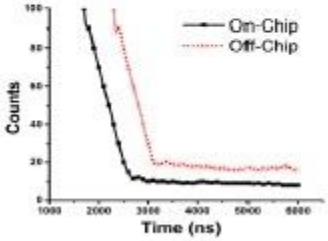


(b)

Fig. 10: Experimental setup for DCR measurement (a), and the measured noise rate vs threshold for APD1 and APD2 (b).



(a)



(b)

Fig. 11: After-pulse measurement: (a) the distribution of the time interval between two consecutive dark pulses for APD1 (a) and with room in steady-state (b).

D. *Noise Characteristics*

High-power dissipation can drift the breakdown voltage, and change the SPAD response regarding to the detection efficiency and noise. Delayed release of trapped charges due to the large charge trapping in SPAD can also retrigger the detector and cause after-pulsing. After-pulsing causes a non-linear distortion in photon-counting. Decreasing the avalanche-time duration has reduced the power-dissipation, charge-trapping and the optical crosstalk due to the minimization of the hot-carrier emission. The noise characteristics have been studied based on the Dark-Count Rate (DCR) and After-pulsing. In order to reduce the excess-noise and be able to detect high-rate array of photons, the dead-time is minimized. The electronic setup for DCR measurement is shown in Fig. 10(a).

Here the SiAPD is placed into a thermally stabilized light-tight box and the number of noise-pulses generated per unit time is measured as a function of the discriminator threshold. The results are shown in Fig. 10(b). It offers a timing resolution of 50 ps and a dark-count of 14000 c/s at an excess bias voltage of 1 V at room temperature. Here the threshold is normalized to the one-photon signal amplitude [28]. The after-pulse noise measurement results are shown in Fig. 11 (applied set-up as [30]).

The amplified signal is passed to the discriminator that generates two fast logic outputs which in turn, are appropriately delayed, with one used as start and the other as stop of the time-to-amplitude converter (TAC). After a precision calibration of the time scale a delay configuration is chosen to have a self-coincidence peak below the overall TAC threshold, and thus the system was only triggered whenever, following the main signal, there was another pulse between 50 ns and the full time range. In these conditions, the distribution of time intervals between two consecutive signals is measured [28]. The results demonstrate that the implemented CMQC has reduced the after-pulses.

E. *Effects of On-Chip Integration*

The resistance and capacitance of SiAPD, quenching circuit, silicon substrate, and resistive load all affect on the efficiency and response time of the GM-SiAPD. Significant effort is required to reduce the offsets, tune and adapt the connection between SiAPD and the photon-counter circuitry using bulky resistors and capacitors. This off-chip wiring imposes a dramatic noise and power-distortion to the system, limits the efficiency and sensitivity of the whole detector front-end. In order to overcome these drawbacks and limits, here we have integrated on-chip the introduced photon-counter with implemented SiAPDs, towards offering a more miniaturized detector front-end with higher sensitivity and maximum efficiency.

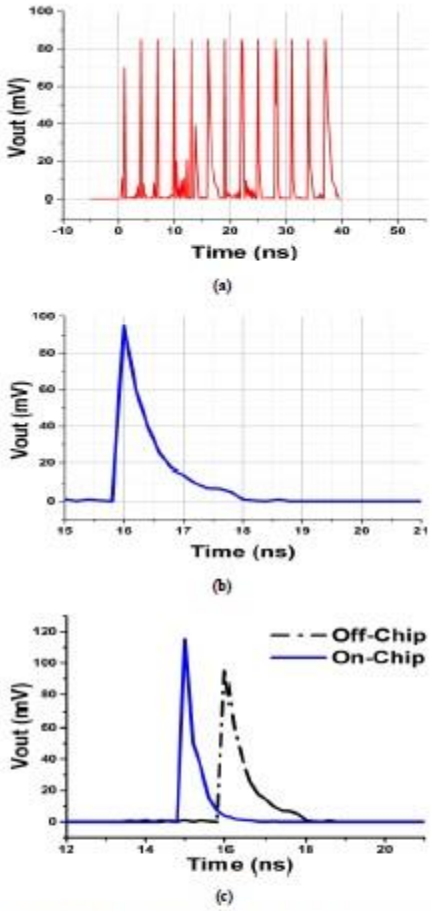


Fig. 12: The Scope capture of single-photon events (a), and close-up view of a single event (b). Comparison of off-chip and on-chip integrated photon counter responses (c).

Figure 12 (a) shows the scope capture of the single photon events during 40 ns. The close-up view of a single event for on-chip and off-chip SiAPDs are shown in Figs. 12(b)-(c) respectively. The results show that on-chip integration of the APD and photon-counting circuitry has reduced the after-pulsing and increased the sensitivity accompanied with significantly lower-power consumption.

The main characteristics of the implemented photon-counters are summarized in Tables 4-5. The comparison of off-chip and on-chip integrated photon-counter responses (Fig. 12(c)) shows a higher SNR in additional to a faster response (2-5 ns).

Table 4: Characteristics of the Implemented Quench Techniques

Ref	Operation Voltage Level	Power Diss. (mW)	Quench-Time (ns)	Dead-Time (ns)	Size (mm²)
PQ*	1.8/3 V	1.3	250µs	90	2
AQ*	1.8/3 V	0.9	200ns	60	1.1
MQ*	1.8/3 V	0.2	30ns	10	1.5
CMQ*	1.8 V	0.4	10ns	2	0.1
CMQ-APD*	1.8 V	0.1	8ns	2	0.1

*The results measurements are based on bare dye wafer (The values for packaged IC were variable up to 10%-50% higher)

Table 5: Comparison of the implemented CMQC technique with other works

Ref	Technology (µm)	Supply Voltage	Power (mW)	Quench-Time (ns)	Reset Time (ns)	T_d-- (ns)	T_hold* (ns)	Hold-off Control
[2]	0.35	3.3 V		9	12	40	5-660	FPGA
[9]	0.8	20	20	25	20	50	5-500	No
[10]--	0.35	3.5	20	1	5µs	-	-	No
[31]	0.8	10 V	20	100		20		No
[32]	0.35	5	-	-	2	40	40-2000	Yes
[33]	0.35	6		1	3		-	No
CMQ	0.18	1.8 V	0.4	3-10	1	2	1-5000	Yes

* Hold-off time **Simulation ***Dead-time

VI. Conclusion

In order to operate the SiAPD in Geiger mode for single-photon counting, a new high-speed, low-power and controllable photon-counting system was reported in this paper using standard CMOS technology. It includes an integrated hold-off time control and on-chip counter in a small area with a fast quench-rest time, low-power consumption and low-noise characteristics. It exhibits a quench-time of 3-10ns, a controllable hold-off time in 1ns-5µs, and maximum power consumption of 0.6mW. Decreasing the avalanche-time duration has reduced the power-dissipation, charge-trapping (after-pulsing) and the optical cross-talk noise. Characterizing the implemented device in response to single and multiple photon detections show its preference specially regarding to the power-consumption, speed, controllability and size. Integrating the SiAPD and photon-counting circuitry on the same chip offers a fill-factor of 95% with a higher sensitivity, and it has reduced the after-pulsing and power-consumption.

Acknowledgment

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